Chapter 25 The Pipeline Analog to Digital Converter

The Pipeline ADC decides the bits of the output one by one. It first decides the most significant bit and then the second until the least significant bit is decided. Let us assume that the ADC outputs N bits, $b_{N-1}, b_{n-2}, \cdots, b_0$. For any ADC, there will be an input Vin and a Vref. The relationship between Vin, Vref and the outputs bits are always as follows:

$$Vin = \sum_{i=0}^{N-1} b_i 2^i \frac{Vref}{2^N} \tag{2.5-1}$$

Suppose N=3. Then we have the following formula:

$$\begin{aligned} Vin &= \left(b_2 2^2 + b_1 2^1 + b_0 2^0\right)\frac{V_{ref}}{2^3} \\ &= (b_2 \frac{Vref}{2} + b_1 \frac{Vref}{4} + b_0 \frac{Vref}{8}) \end{aligned} \tag{2.5-2}$$

From Equation (2.5-2), we can easily see that if $Vin \geq \frac{Vref}{2}$, b_2 must be set to be 1; otherwise, 0. This is how we can determine the value of b_2.

Once b_2 is determined, we can determine b_1 as follows:

If $b_2=1$, we determine b_1 by comparing $Vin - \frac{Vref}{2}$ with $\frac{Vref}{4}$; otherwise, determine b_1 by comparing Vin with $\frac{Vref}{4}$.

The above discussion can be generalized to N bits and the first subcircuit of the Pipeline ADC is illustrated in Fig. 25-1.

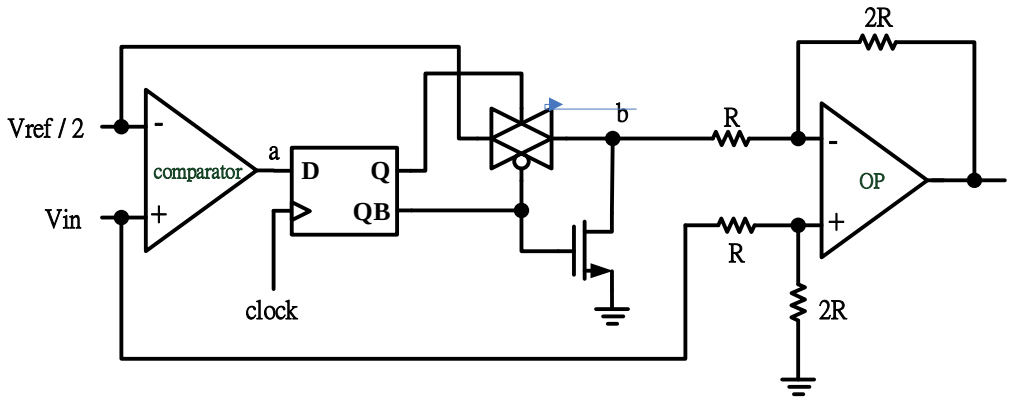


Fig. 25-1 The first stage of the Pipeline ADC

Let us try to understand the circuit in Fig. 25-1. Suppose the ADC has N bits as output. The input of Vin is first compared with Vref/2. There are two cases:

Case 1: Vin is larger than Vref/2, Va will be high and V(Q) will also be high. The high value of V(Q) will cause the transmission gate to work and Vref/2 will be transmitted to Vb. Vb will be Vref/2 and b_N will be set to be 1. The connection of the inputs of the OP makes the OP to function as a subtractor. As can be seen, this output of the OP will be 2 times the difference of the inputs. Thus the output of the first stage is 2(Vin-Vref/2).

Case 2: Vin is smaller than or equal to Vref/2, Va will be low and V(QB) will be high. The high value of V(QB) will cause the transmission gate not to function. Transistor M1 will be short circuited, Vb will be 0 and b_N will set to be 0. The output of the first stage is now 2(Vin-0)=2Vin.

The output of the above circuit will be the input of the second stage of the Pipeline ADC. Therefore, we again have two cases;

Case 1: The output is 2(Vin-Vref/2). In this case, we are going to compare 2(Vin-Vref/2) with Vref/2. If the result is larger than 0, it means (Vin-Vref/2)>Vref/4 and we then set b_{N-1} to be 1; otherwise, we set $b_{N-1}$to be 0.

Case 2: The output is 2(Vin). In this case, we are going to compare 2(Vin) with Vref/2. If the result is larger than 0, it means Vin>Vref/4 and we then set b_{N-1} to be 1; otherwise, we set $b_{N-1}$to be 0.

The Pipeline ADC will have N subcircuits as described in Fig. 25-1. These subcircuits will determine b_N, b_{N-1}, …, b_0 one by one. In Fig. 25-2, we show a Pipeline ADC with 3 output bits.

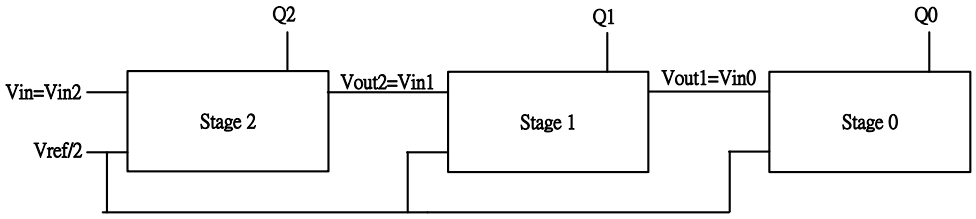


Fig. 25-2 A Pipeline ADC with three output bits

Let us give some examples. In all examples, Vref/2=0.8V.

Example 25-1. Vin=1.5V

In this case, the circuits perform as below.

Stage 2: Since Vin2=1.5V is larger than Vref/2=0.8V, Q2=high and the inputs of the subtractor are V+=1.5V and V-=0.8V. Vout1=2(1.5-0.8)V=1.4V. This will be the input of Stage 1.

Stage 1: Since Vin1=1.4V is larger than Vref/2=0.8V, Q1=high and the inputs of the subtractor are V+=1.4V and V-=0.8V. Vout1=2(1.4-0.8)V=1.2V. This will be the input of Stage 0.

Stage 0: Since Vin1=1.2V is larger than Vref/2=0.8V, Q0=high.

For Vin=1.5V, Q=(high, high, high). The ADC output is (111) which is correct.

Example 25-2 Vin=0.3V**.**

In this case, the circuits perform as below.

Stage 2: Since Vin2=0.3V is smaller than Vref/2=0.8V, Q2=low and the inputs of the subtractor are V+=0.3V and V-=0V. Vout1=2(0.3-0)V=0.6V. This will be the input of Stage 1.

Stage 1: Since Vin1=0.6V is smaller than Vref/2=0.8V, Q1=low and the inputs of the subtractor are V+=0.6V and V-=0V. Vout1=2(0.6-0)V=1.2V. This will be the input of Stage 0.

Stage 0: Since Vin0=1.2V is larger than Vref/2=0.8V, Q0=high.

For Vin=0.3V, Q(low, low, high). The ADC output is (001) which is correct.

Example 25-3 Vin=0.7V

. In this case, the circuits perform as below.

Stage 2: Since Vin2=0.7V is smaller than Vref/2=0.8V, Q2=low and the inputs of the subtractor are V+=0.7V and V-=0V. Vout1=2(0.7-0)V=1.4V. This will be the input of Stage 1.

Stage 1: Since Vin1=1.4V is larger than Vref/2=0.8V, Q1=high and the inputs of the subtractor are V+=1.4V and V-=0.8V. Vout1=2(1.4-0.8)V=1.2V. This will be the input of Stage 0.

Stage 0: Since Vin0=1.2V is larger than Vref/2=0.8V, Q0=high.

For Vin=0.3V, Q(low, high, high). The ADC output is (011) which is correct.

Section 25.1 The Rail to Rail Comparator Circuit

In the Pipeline ADC, the comparator may compare very small and very large numbers. Therefore we use the rail to rail comparator introduced in Chapter 3. The circuit is shown in Fig. 25.1-1.

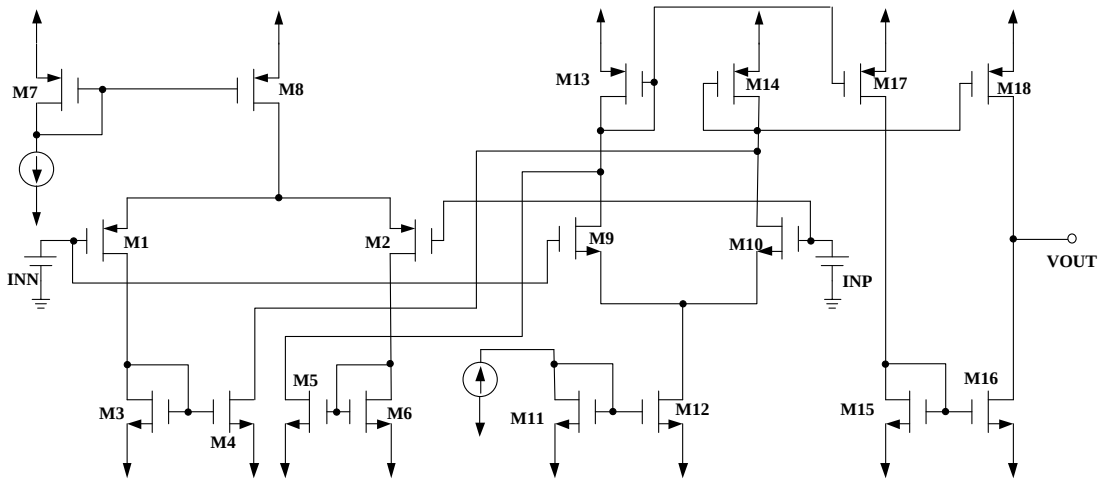


Fig. 25.1-1 The comparator used in the Pipeline ADC.

Experiment 25.1-1 The Testing of the Rail to Rail Comparator

The program of this experiment is in Table 25.1-1 and the results are in Fig. 25.1-2. As can be seen, this comparator works correctly

Table 25.1-1 The program for Experiment 25.1-1

```
Rail_to_Rail_Comparator
.PROTECT
.OPTION POST
.lib "d:\model\tsmc\MIXED035\mm0355v.l" TT
.UNPROTECT
.op

M6        N1N322 N1N322 VSS VSS    NCH L=2U W=3U M=2
M3        N1N320 N1N320 VSS VSS    NCH L=2U W=3U M=2
M8        VVG I2U_S VDD VDD    PCH L=5U W=6U M=2
M1       N1N320 INN VVG VDD    PCH L=2U W=6U M=2
M2       N1N322 INP VVG VDD    PCH L=2U W=6U M=2
```

```
M7         I2U_S I2U_S VDD VDD    PCH L=5U W=6U M=2
M5      N1N365 N1N322 VSS VSS    NCH L=2U W=3U M=2
M4      N1N362 N1N320 VSS VSS    NCH L=2U W=3U M=2

M10     N1N362 INP N1N372 VSS    NCH L=2U W=3U M=2
M11     I2U I2U VSS VSS    NCH L=5U W=5U M=2
M12     N1N372 I2U VSS VSS    NCH L=5U W=5U M=2
M9      N1N365 INN N1N372 VSS    NCH L=2U W=3U M=2
M14     N1N362 N1N362 VDD VDD    PCH L=2U W=6U M=2
M13     N1N365 N1N365 VDD VDD    PCH L=2U W=6U M=2

M17     N1N431 N1N365 VDD VDD    PCH L=2U W=6U M=2
M18     VOUT N1N362 VDD VDD    PCH L=2U W=6U M=2
M15     N1N431 N1N431 VSS VSS    NCH L=2U W=3U M=2
M16     VOUT N1N431 VSS VSS    NCH L=2U W=3U M=2

vdd vdd gnd 1.6
vss vss gnd -1.6
v01 inn gnd 0.8
v02 inp gnd pwl(0 -1.5 0.5m 1.5 1m -1.5)
i01 i2u_s vss 2u
i02 vdd i2u 2u

.tran 0.1u 1m
.probe v(VOUT)

.END
```

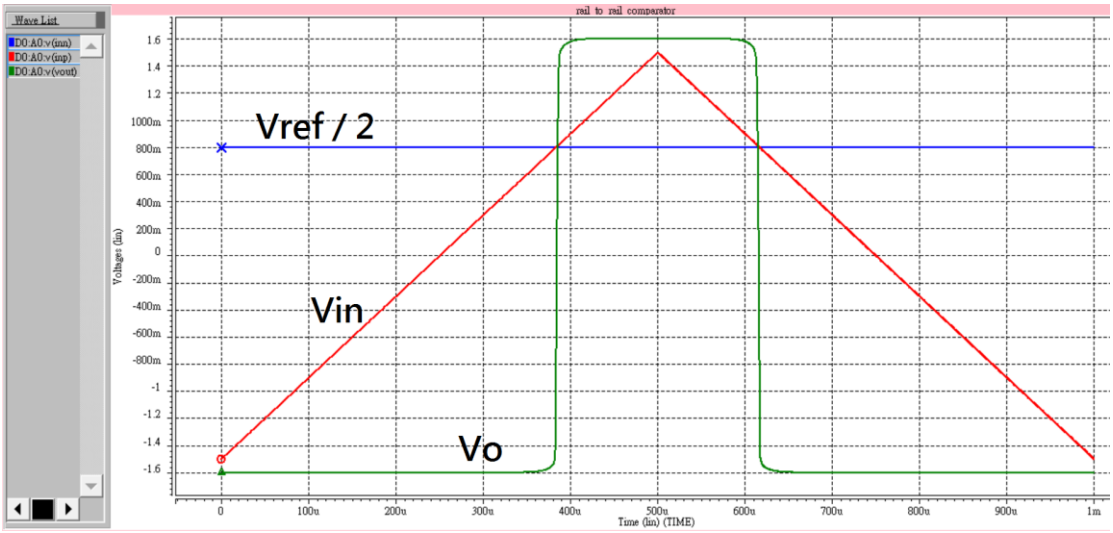


Fig. 25.1-2 The results of Experiment 25.1-1

Section 25.2 The Connection of the Comparator with DFF and Non-overlapped Clock Generator

The Pipeline ADC needs a DFF and a non-overlapping clock generator. This DFF is connected to the output of a comparator. These circuits are shown in Fig. 25.2-1

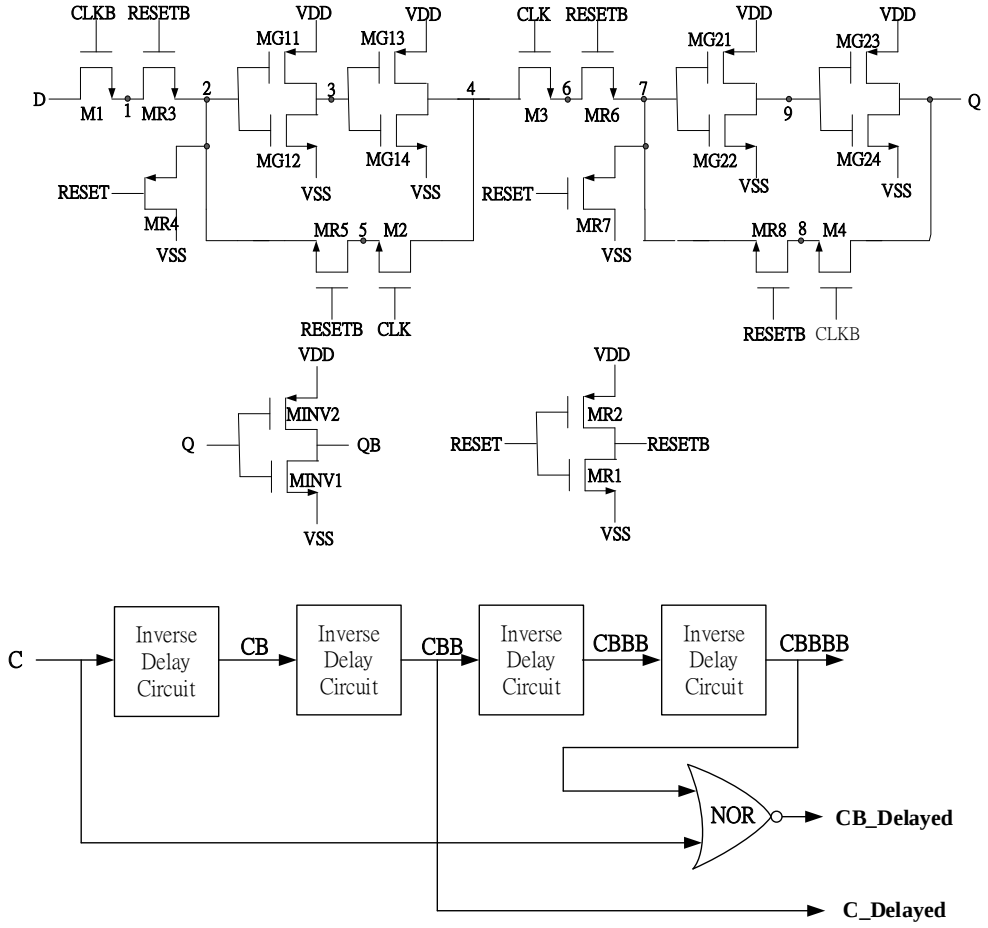


Fig. 25.2-1 DFF and non-overlapped clock generator

Fig. 25.2-2 shows the connection of the comparator, the DFF and the clock.

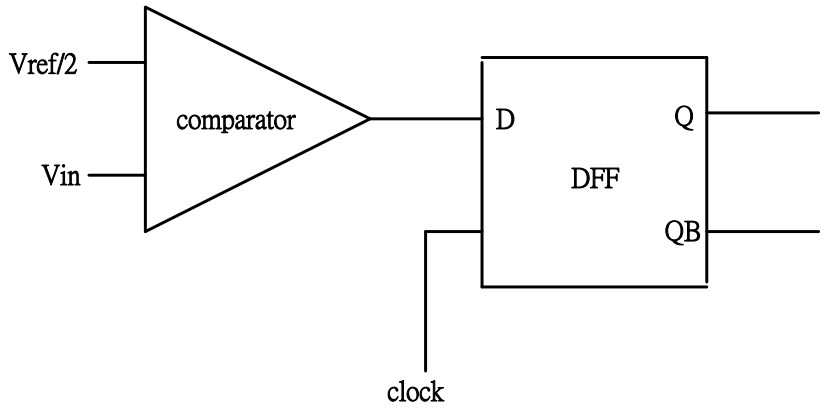


Fig. 25.2-2 the comparator, the DFF and the clock

Experiment 25.2-1 The First Test of the DFF Circuit

The program of this experiment is in Table 25.2-1 and the results are shown in Fig. 25.2-3.

Table 25.2-1 The program for Experiment 25.2-1

```
Test of comparator and DFF
.PROTECT
.OPTION POST
.lib "d:\model\tsmc\MIXED035\mm0355v.l" TT
.UNPROTECT
.op

.subckt comparator INP INN VOUT I2U I2U_S VDD VSS
M6        N1N322 N1N322 VSS VSS    NCH L=2U W=3U M=2
M3        N1N320 N1N320 VSS VSS    NCH L=2U W=3U M=2
M8        VVG I2U_S VDD VDD    PCH L=5U W=6U M=2
M1      N1N320 INN VVG VDD    PCH L=2U W=6U M=2
M2      N1N322 INP VVG VDD    PCH L=2U W=6U M=2
M7        I2U_S I2U_S VDD VDD    PCH L=5U W=6U M=2
M5     N1N365 N1N322 VSS VSS    NCH L=2U W=3U M=2
M4     N1N362 N1N320 VSS VSS    NCH L=2U W=3U M=2

M10     N1N362 INP N1N372 VSS    NCH L=2U W=3U M=2
M11     I2U I2U VSS VSS    NCH L=5U W=5U M=2
M12     N1N372 I2U VSS VSS    NCH L=5U W=5U M=2
M9     N1N365 INN N1N372 VSS    NCH L=2U W=3U M=2
```

```
M14     N1N362 N1N362 VDD VDD    PCH L=2U W=6U M=2
M13     N1N365 N1N365 VDD VDD    PCH L=2U W=6U M=2

M17     N1N431 N1N365 VDD VDD    PCH L=2U W=6U M=2
M18     VOUT N1N362 VDD VDD    PCH L=2U W=6U M=2
M15     N1N431 N1N431 VSS VSS    NCH L=2U W=3U M=2
M16     VOUT N1N431 VSS VSS    NCH L=2U W=3U M=2
.ends

.subckt DFF CLK CLKB RESET D Q QB VDD VSS
MR1       RESETB  RESET     VSS  VSS  NCH W=50u    L=1u
MR2 RESETB    RESET     VDD VDD PCH  W=50u    L=1u

M1        D     CLKB      1     VSS  NCH W=50u    L=1u
MR3       1     RESETB    2     VSS  NCH W=50u    L=1u

MR4       2     RESET     VSS  VSS  NCH W=50u    L=1u

MG11      3     2     VDD VDD PCH  W=50u    L=1u
MG12      3     2     VSS  VSS  NCH W=50u    L=1u
MG13      4     3     VDD VDD PCH  W=50u    L=1u
MG14      4     3     VSS  VSS  NCH W=50u    L=1u

M2        4     CLK  5     VSS  NCH W=50u    L=1u
MR5       5     RESETB    2     VSS  NCH W=50u    L=1u

M3        4     CLK  6     VSS  NCH W=50u    L=1u
MR6       6     RESETB    7     VSS  NCH W=50u    L=1u

MR7       7     RESET     VSS  VSS  NCH W=50u    L=1u

MG21      9     7     VDD VDD PCH  W=50u    L=1u
MG22      9     7     VSS  VSS  NCH W=50u    L=1u
MG23      Q     9     VDD VDD PCH  W=50u    L=1u
MG24      Q     9     VSS  VSS  NCH W=50u    L=1u

M4        Q     CLKB      8     VSS  NCH W=50u    L=1u
MR8       7     RESETB    8     VSS  NCH W=50u    L=1u
```

```
MINV1    QB          Q           VSS VSS  NCH W=50u    L=1u
MINV2    QB          Q           VDD      VDD PCH  W=50u    L=1u
.ends

.subckt INV1 IN OUT VDD VSS
M1       OUT      IN          VDD      VDD      PCH       W=2U      L=1U
M2       OUT      IN          VSS      VSS      NCH       W=1U      L=1U
.ends

.subckt INV2 IN OUT VDD VSS
M1       OUT      IN          VDD      VDD      PCH       W=100U      L=2U
M2       OUT      IN          VSS      VSS      NCH       W=50U      L=2U
.ends

.subckt NOR A B OUT VDD VSS
M1       1        A           VDD      VDD      PCH       W=100U      L=2U
M2       OUT      B           1        VDD      PCH       W=100U      L=2U
M3       OUT      B           VSS      VSS      NCH       W=50U      L=2U
M4       OUT      A           VSS      VSS      NCH       W=50U      L=2U
.ends

.subckt NOVLP_CLK C C_Delayed CB_Delayed VDD VSS
X1 C CB VDD VSS INV1
X2 CB CBB VDD VSS INV2
X3 CBB CBBB VDD VSS INV1
X4 CBBB CBBBB VDD VSS INV2
R1 CBB C_Delayed 0
X7 C CBBBB CB_Delayed VDD VSS NOR
.ends

X1 vin vref a I2U I2U_S VDD VSS comparator
X2 CLK CLK_delayed CLKB_delayed VDD VSS NOVLP_CLK
X3 CLK_delayed CLKB_delayed RESET a Q QB VDD VSS DFF

vdd vdd 0 1.6
vss vss 0 -1.6
```

```
vref vref 0 0.8
vin vin 0 1.0

i01 i2u_s vss 2u
i02 vdd i2u 2u

Vclk  CLK   0      pulse(-1.6v 1.6v    1.1us 0.01us 0.01us 0.13us 0.26us)
Vreset      RESET      0      pulse(-1.6v 1.6v    0us 0.01us 0.01us 1us 20ms)

.tran 10ns          30us

.END
```

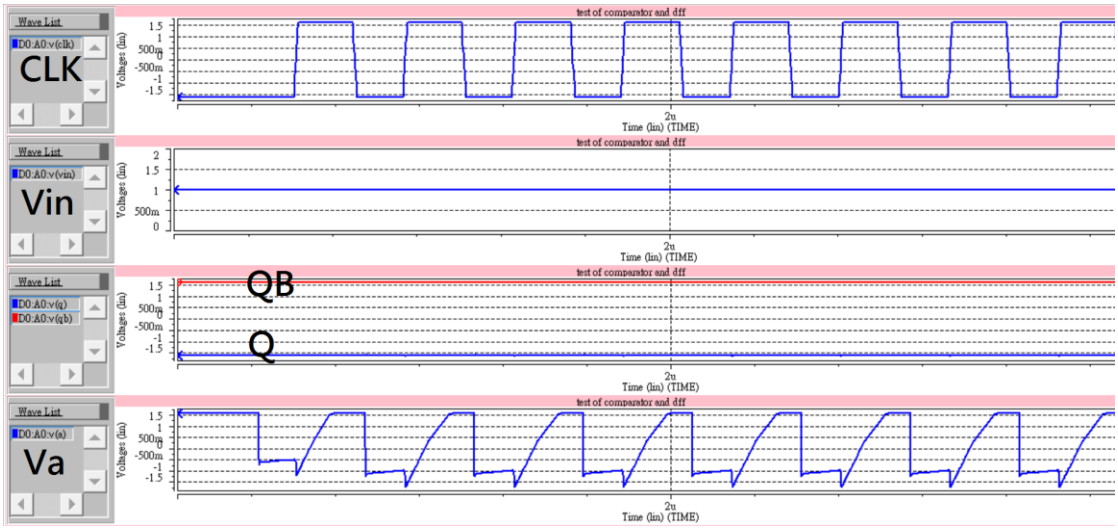


Fig. 25.2-3 The results of the Experiment 25.2-1

We can see that there are problems. Consider Fig. 25.2-1. Va is obviously influenced by the signal CLKB which should not happen. This is due to the fact that the parasitic capacitor between the drain and gate of transistor M1 in D-flip-flop is too large. This causes the output of the comparator to be coupled by the clock signal CLKB.

To understand how the parasitic capacitance influences the circuit, we slightly modified the circuit by inserting a resistor with value 0 into the circuit as shown in Fig. 25.2-4.

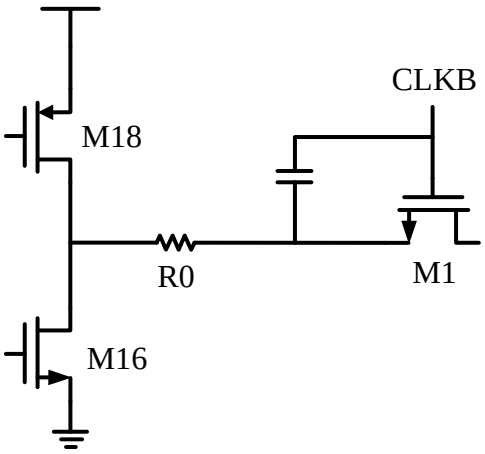


Fig. 25.2-4 A slight modification of the circu

Experiment 25.2-2 A Testing of the Parasitic Capacitor

In this experiment, we test the circuit with the resistor RO inserted. The program is Table 25.2-2 and the results are in Fig. 25.2-5.

Table 25.2-2 The program of Experiment 25.2-2

```
Test of comparator and DFF
.PROTECT
.OPTION POST
.lib "d:\model\tsmc\MIXED035\mm0355v.l" TT
.UNPROTECT
.op

.subckt comparator INP INN VOUT I2U I2U_S VDD VSS
M6        N1N322 N1N322 VSS VSS    NCH L=2U W=3U M=2
M3        N1N320 N1N320 VSS VSS    NCH L=2U W=3U M=2
M8        VVG I2U_S VDD VDD    PCH L=5U W=6U M=2
M1       N1N320 INN VVG VDD    PCH L=2U W=6U M=2
M2       N1N322 INP VVG VDD    PCH L=2U W=6U M=2
M7        I2U_S I2U_S VDD VDD    PCH L=5U W=6U M=2
M5     N1N365 N1N322 VSS VSS    NCH L=2U W=3U M=2
M4     N1N362 N1N320 VSS VSS    NCH L=2U W=3U M=2

M10     N1N362 INP N1N372 VSS    NCH L=2U W=3U M=2
```

```
M11     I2U I2U VSS VSS    NCH L=5U W=5U M=2
M12     N1N372 I2U VSS VSS    NCH L=5U W=5U M=2
M9     N1N365 INN N1N372 VSS    NCH L=2U W=3U M=2
M14     N1N362 N1N362 VDD VDD    PCH L=2U W=6U M=2
M13     N1N365 N1N365 VDD VDD    PCH L=2U W=6U M=2

M17     N1N431 N1N365 VDD VDD    PCH L=2U W=6U M=2
M18     VOUT N1N362 VDD VDD    PCH L=2U W=6U M=2
M15     N1N431 N1N431 VSS VSS    NCH L=2U W=3U M=2
M16     VOUT N1N431 VSS VSS    NCH L=2U W=3U M=2
.ends

.subckt DFF CLK CLKB RESET D Q QB VDD VSS
MR1       RESETB      RESET    VSS VSS NCH      W=50u    L=1u
MR2      RESETB RESET    VDD      VDD      PCHW=50u    L=1u

M1        D     CLKB     1     VSS NCH      W=50u    L=1u
MR3       1     RESETB 2     VSS NCH      W=50u    L=1u

MR4       2     RESET    VSS VSS NCH      W=50u    L=1u

MG11     3     2     VDD      VDD      PCHW=50u    L=1u
MG12     3     2     VSS VSS NCH      W=50u    L=1u
MG13     4     3     VDD      VDD      PCHW=50u    L=1u
MG14     4     3     VSS VSS NCH      W=50u    L=1u

M2        4     CLK      5     VSS NCH      W=50u    L=1u
MR5       5     RESETB 2     VSS NCH      W=50u    L=1u

M3        4     CLK      6     VSS NCH      W=50u    L=1u
MR6       6     RESETB 7     VSS NCH      W=50u    L=1u

MR7       7     RESET    VSS VSS NCH      W=50u    L=1u

MG21     9     7     VDD      VDD      PCHW=50u    L=1u
MG22     9     7     VSS VSS NCH      W=50u    L=1u
MG23     Q     9     VDD      VDD      PCHW=50u    L=1u
MG24     Q     9     VSS VSS NCH      W=50u    L=1u
```

```
M4      Q    CLKB    8    VSS NCH      W=50u   L=1u
MR8     7    RESETB  8    VSS NCH      W=50u   L=1u

MINV1   QB       Q        VSS    VSS NCH      W=50u   L=1u
MINV2   QB       Q        VDD    VDD      PCHW=50u   L=1u
.ends

.subckt INV1 IN OUT VDD VSS
M1      OUT     IN          VDD     VDD     PCH      W=2U     L=1U
M2      OUT     IN          VSS     VSS     NCH      W=1U     L=1U
.ends

.subckt INV2 IN OUT VDD VSS
M1      OUT     IN          VDD     VDD     PCH      W=100U     L=2U
M2      OUT     IN          VSS     VSS     NCH      W=50U      L=2U
.ends

.subckt NOR A B OUT VDD VSS
M1      1       A          VDD     VDD     PCH      W=100U     L=2U
M2      OUT     B           1      VDD     PCH      W=100U     L=2U
M3      OUT     B          VSS     VSS     NCH      W=50U      L=2U
M4      OUT     A          VSS     VSS     NCH      W=50U      L=2U
.ends

.subckt NOVLP_CLK C C_Delayed CB_Delayed VDD VSS
X1 C CB VDD VSS INV1
X2 CB CBB VDD VSS INV2
X3 CBB CBBB VDD VSS INV1
X4 CBBB CBBBB VDD VSS INV2
R1 CBB C_Delayed 0
X7 C CBBBB CB_Delayed VDD VSS NOR
.ends

X1 vin vref a I2U I2U_S VDD VSS comparator
X2 CLK CLK_delayed CLKB_delayed VDD VSS NOVLP_CLK
X3 CLK_delayed CLKB_delayed RESET a_tmp Q QB VDD VSS DFF
```

```
R0 a_tmp a 0

vdd vdd 0 1.6
vss vss 0 -1.6

vref vref 0 0.8
vin vin 0 1.0

i01 i2u_s vss 2u
i02 vdd i2u 2u

VclkCLK       0      pulse(-1.6v 1.6v    1.1us 0.01us 0.01us 0.13us 0.26us)
Vreset     RESET    0      pulse(-1.6v 1.6v    0us 0.01us 0.01us 1us 20ms)

.tran 10ns          30us
.probe I(R0) I(X1.M16) I(X1.M18)
.END
```

Fig. 25.2-5 shows that there is a current flowing through the resistor. This current is caused by the parasitic capacitor and should not exist. The existence of this current explains why the output of the comparator is influenced by the clock.

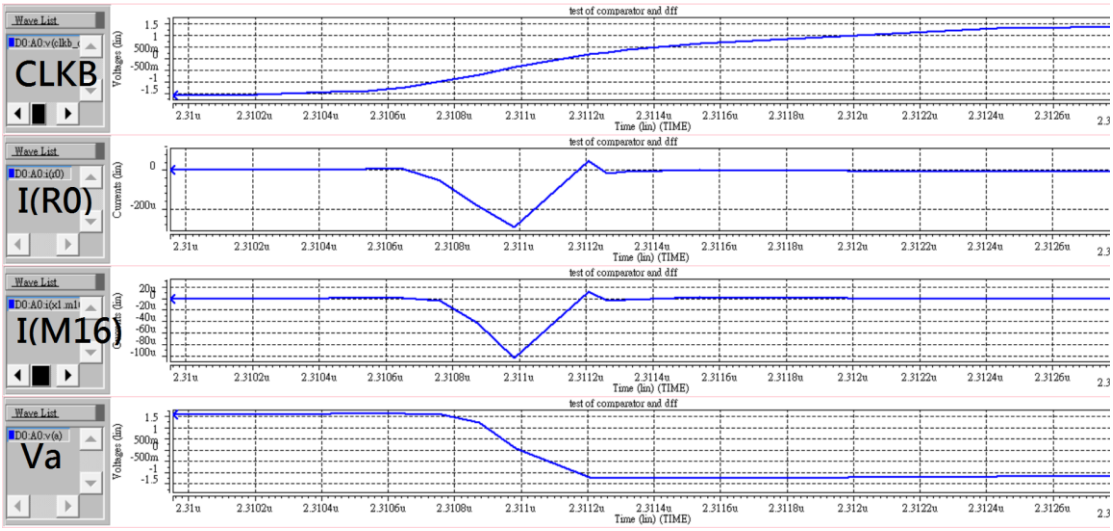


Fig. 25.2-5 The existence of current through the parasitic capacitance

Experiment 25.2-3 The Testing the Circuit Involving the Comparator and the DFF after Reducing the Gate Size of the M1 Transistor

To reduce the current as described above, we reduced the gate of the transistor M1. Vin =0.1V. The program is in Table 25.2-2 and the results are in Fig. 25.2-6.

Table 25.2-23 The program for Experiment 25.2-2

```
Test of comparator and DFF
.PROTECT
.OPTION POST
.lib "d:\model\tsmc\MIXED035\mm0355v.l" TT
.UNPROTECT
.op

.subckt comparator INP INN VOUT I2U I2U_S VDD VSS
M6         N1N322 N1N322 VSS VSS    NCH L=2U W=3U M=2
M3         N1N320 N1N320 VSS VSS    NCH L=2U W=3U M=2
M8         VVG I2U_S VDD VDD    PCH L=5U W=6U M=2
M1       N1N320 INN VVG VDD    PCH L=2U W=6U M=2
M2       N1N322 INP VVG VDD    PCH L=2U W=6U M=2
M7         I2U_S I2U_S VDD VDD    PCH L=5U W=6U M=2
M5     N1N365 N1N322 VSS VSS    NCH L=2U W=3U M=2
M4     N1N362 N1N320 VSS VSS    NCH L=2U W=3U M=2

M10     N1N362 INP N1N372 VSS    NCH L=2U W=3U M=2
M11     I2U I2U VSS VSS    NCH L=5U W=5U M=2
M12     N1N372 I2U VSS VSS    NCH L=5U W=5U M=2
M9     N1N365 INN N1N372 VSS    NCH L=2U W=3U M=2
M14     N1N362 N1N362 VDD VDD    PCH L=2U W=6U M=2
M13     N1N365 N1N365 VDD VDD    PCH L=2U W=6U M=2

M17     N1N431 N1N365 VDD VDD    PCH L=2U W=6U M=2
M18     VOUT N1N362 VDD VDD    PCH L=2U W=6U M=2
M15     N1N431 N1N431 VSS VSS    NCH L=2U W=3U M=2
M16     VOUT N1N431 VSS VSS    NCH L=2U W=3U M=2
.ends

.subckt DFF CLK CLKB RESET D Q QB VDD VSS
MR1        RESETB   RESET      VSS  VSS   NCH W=5u      L=1u
MR2 RESETB    RESET      VDD VDD PCH  W=5u      L=1u
```

```
M1      D    CLKB     1    VSS  NCH W=5u    L=1u
MR3     1    RESETB   2    VSS  NCH W=5u    L=1u

MR4     2    RESET    VSS  VSS  NCH W=5u    L=1u

MG11    3    2    VDD VDD PCH  W=5u    L=1u
MG12    3    2    VSS  VSS  NCH W=5u    L=1u
MG13    4    3    VDD VDD PCH  W=5u    L=1u
MG14    4    3    VSS  VSS  NCH W=5u    L=1u

M2      4    CLK  5    VSS  NCH W=5u    L=1u
MR5     5    RESETB   2    VSS  NCH W=5u    L=1u

M3      4    CLK  6    VSS  NCH W=5u    L=1u
MR6     6    RESETB   7    VSS  NCH W=5u    L=1u

MR7     7    RESET    VSS  VSS  NCH W=5u    L=1u

MG21    9    7    VDD VDD PCH  W=5u    L=1u
MG22    9    7    VSS  VSS  NCH W=5u    L=1u
MG23    Q    9    VDD VDD PCH  W=5u    L=1u
MG24    Q    9    VSS  VSS  NCH W=5u    L=1u

M4      Q    CLKB     8    VSS  NCH W=5u    L=1u
MR8     7    RESETB   8    VSS  NCH W=5u    L=1u

MINV1   QB       Q        VSS VSS  NCH W=5u    L=1u
MINV2   QB       Q        VDD      VDD PCH  W=5u    L=1u
.ends

.subckt INV1 IN OUT VDD VSS
M1      OUT     IN       VDD     VDD     PCH      W=2U     L=1U
M2      OUT     IN       VSS     VSS     NCH      W=1U     L=1U
.ends

.subckt INV2 IN OUT VDD VSS
M1      OUT     IN       VDD     VDD     PCH      W=10U    L=2U
M2      OUT     IN       VSS     VSS     NCH      W=5U     L=2U
```

```
.ends

.subckt NOR A B OUT VDD VSS
M1      1       A       VDD     VDD     PCH     W=10U     L=2U
M2      OUT     B       1       VDD     PCH     W=10U     L=2U
M3      OUT     B       VSS     VSS     NCH     W=5U      L=2U
M4      OUT     A       VSS     VSS     NCH     W=5U      L=2U
.ends

.subckt NOVLP_CLK C C_Delayed CB_Delayed VDD VSS
X1 C CB VDD VSS INV1
X2 CB CBB VDD VSS INV2
X3 CBB CBBB VDD VSS INV1
X4 CBBB CBBBB VDD VSS INV2
R1 CBB C_Delayed 0
X7 C CBBBB CB_Delayed VDD VSS NOR
.ends

X1 vin vref a I2U I2U_S VDD VSS comparator
X2 CLK CLK_delayed CLKB_delayed VDD VSS NOVLP_CLK
X3 CLK_delayed CLKB_delayed RESET a_tmp Q QB VDD VSS DFF

R0 a_tmp a 0

vdd vdd 0 1.6
vss vss 0 -1.6

vref vref 0 0.8
vin vin 0 0.1

i01 i2u_s vss 2u
i02 vdd i2u 2u

Vclk  CLK  0      pulse(-1.6v 1.6v    1.1us 0.01us 0.01us 0.13us 0.26us)
Vreset     RESET      0      pulse(-1.6v 1.6v    0us 0.01us 0.01us 1us 20ms)

.tran 10ns          30us
.probe I(R0) I(X1.M16)
```

```
.END
```

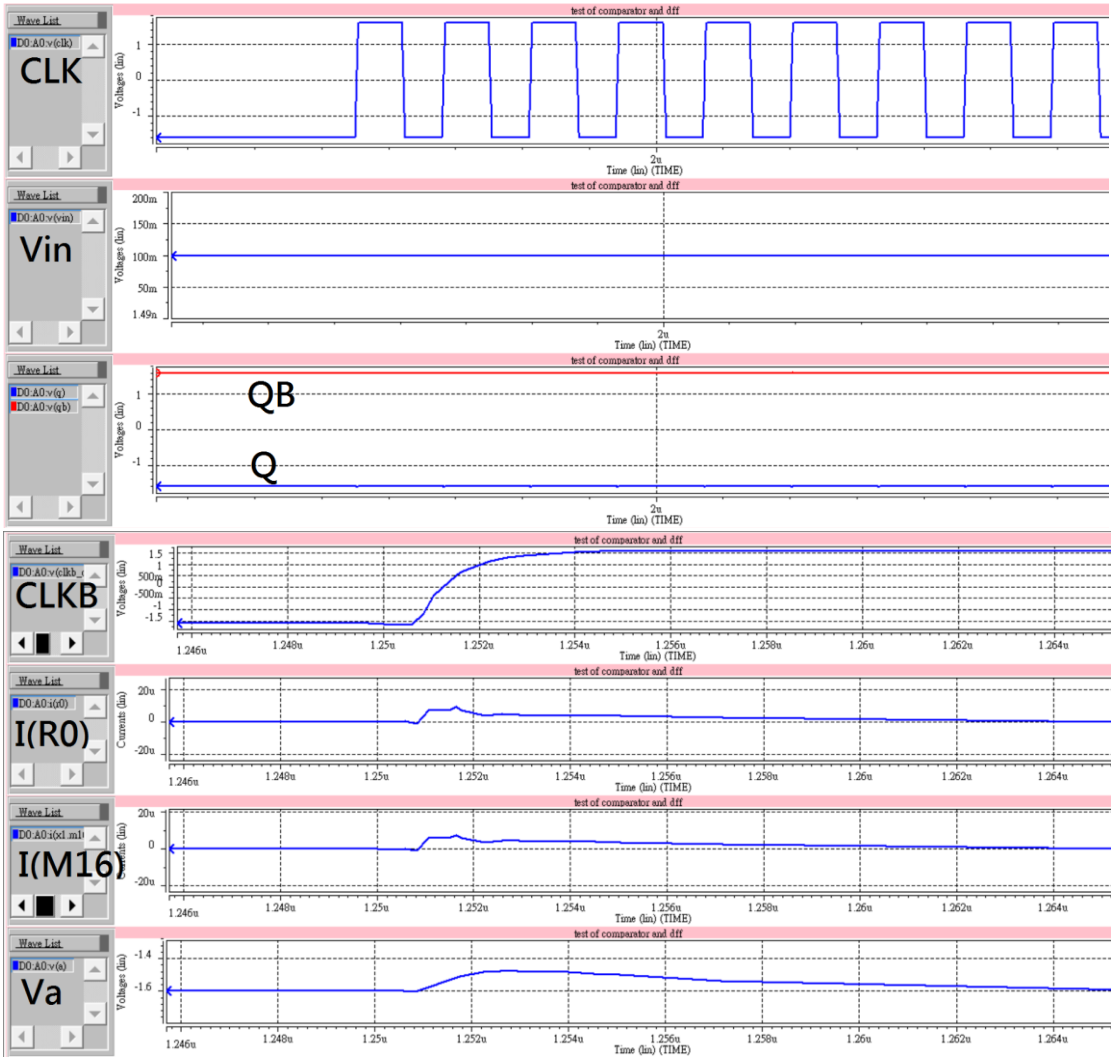


Fig. 25.2-6 Results of Experiment 25.2-2 when Vin=0.1V

Note that the current through the resistor is greatly reduced. Because Vin=0.1V is smaller than Vref/2=0.8V, Q=low and QB=high. The result is correct.

We then tested Vin=1.0V. The results are in Fig. 25.2-7.

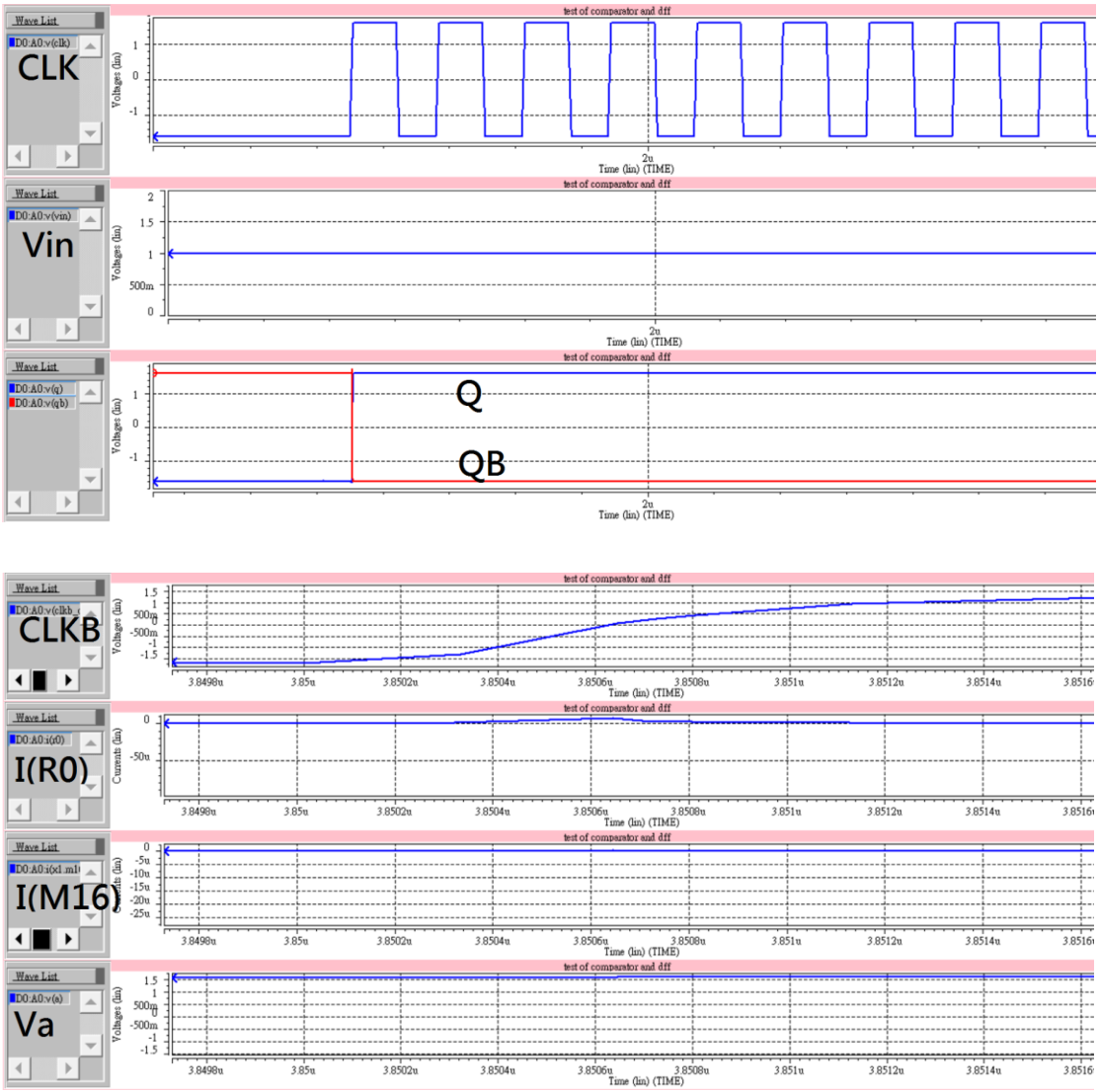


Fig. 25.2-7 The results of Experiment 25.2-2 when Vin=1.0V

Because Vin=1.0V is larger than Vref/2=0.8V, Q=high and QB=low. Besides, the currents have become very small

Section 25.3 The Testing of Comparator, Flip-Flop and the Transmission Gate

The transmission gate is shown in Fig. 25.3-1.

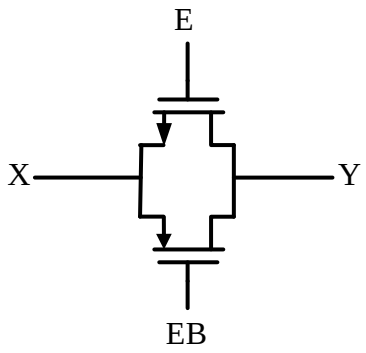


Fig. 25.3-1 The transmission gate circuit.

The circuit involving comparator, flip flop and transmission gate is shown in Fig. 25.3-2 .

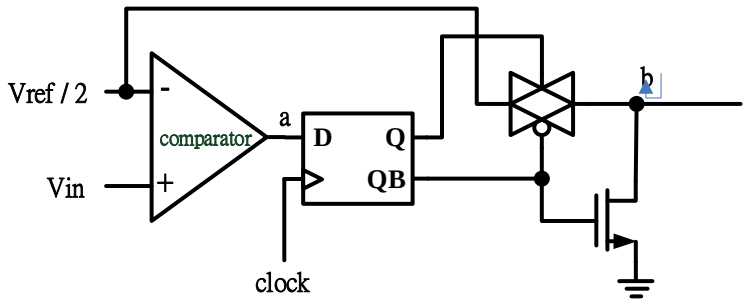


Fig. 25.3-2 The circuit involving comparator, flip flop and transmission gate

Experiment 25.3-1 The Testing of Comparator , D Flip-Flop and Transmission Gate.

The program of this experiment is in Table 25.3-1. In the first test, Vin=0.1V. The results are in Fig. 25.3-3

Table 25.3-1 The program for the first test of Experiment 25.3-1

```
Test of comparator and DFF
.PROTECT
.OPTION POST
```

```
.lib "d:\model\tsmc\MIXED035\mm0355v.l" TT
.UNPROTECT
.op

.subckt comparator INP INN VOUT I2U I2U_S VDD VSS
M6          N1N322 N1N322 VSS VSS    NCH L=2U W=3U M=2
M3          N1N320 N1N320 VSS VSS    NCH L=2U W=3U M=2
M8          VVG I2U_S VDD VDD    PCH L=5U W=6U M=2
M1        N1N320 INN VVG VDD    PCH L=2U W=6U M=2
M2        N1N322 INP VVG VDD    PCH L=2U W=6U M=2
M7          I2U_S I2U_S VDD VDD    PCH L=5U W=6U M=2
M5      N1N365 N1N322 VSS VSS    NCH L=2U W=3U M=2
M4      N1N362 N1N320 VSS VSS    NCH L=2U W=3U M=2

M10      N1N362 INP N1N372 VSS    NCH L=2U W=3U M=2
M11      I2U I2U VSS VSS    NCH L=5U W=5U M=2
M12      N1N372 I2U VSS VSS    NCH L=5U W=5U M=2
M9      N1N365 INN N1N372 VSS    NCH L=2U W=3U M=2
M14      N1N362 N1N362 VDD VDD    PCH L=2U W=6U M=2
M13      N1N365 N1N365 VDD VDD    PCH L=2U W=6U M=2

M17      N1N431 N1N365 VDD VDD    PCH L=2U W=6U M=2
M18      VOUT N1N362 VDD VDD    PCH L=2U W=6U M=2
M15      N1N431 N1N431 VSS VSS    NCH L=2U W=3U M=2
M16      VOUT N1N431 VSS VSS    NCH L=2U W=3U M=2
.ends

.subckt DFF CLK CLKB RESET D Q QB VDD VSS
MR1         RESETB   RESET      VSS  VSS   NCH W=5u      L=1u
MR2 RESETB    RESET      VDD VDD PCH  W=5u      L=1u

M1          D      CLKB       1      VSS   NCH W=5u      L=1u
MR3       1      RESETB    2      VSS   NCH W=5u      L=1u

MR4       2      RESET      VSS  VSS   NCH W=5u      L=1u

MG11      3      2      VDD VDD PCH  W=5u      L=1u
MG12      3      2      VSS  VSS   NCH W=5u      L=1u
```

```
MG13    4    3    VDD VDD PCH  W=5u    L=1u
MG14    4    3    VSS  VSS  NCH W=5u    L=1u

M2      4    CLK  5    VSS  NCH W=5u    L=1u
MR5     5    RESETB  2    VSS  NCH W=5u    L=1u

M3      4    CLK  6    VSS  NCH W=5u    L=1u
MR6     6    RESETB  7    VSS  NCH W=5u    L=1u

MR7     7    RESET    VSS  VSS  NCH W=5u    L=1u

MG21    9    7    VDD VDD PCH  W=5u    L=1u
MG22    9    7    VSS  VSS  NCH W=5u    L=1u
MG23    Q    9    VDD VDD PCH  W=5u    L=1u
MG24    Q    9    VSS  VSS  NCH W=5u    L=1u

M4      Q    CLKB     8    VSS  NCH W=5u    L=1u
MR8     7    RESETB   8    VSS  NCH W=5u    L=1u

MINV1   QB       Q        VSS VSS  NCH W=5u    L=1u
MINV2   QB       Q        VDD      VDD PCH  W=5u    L=1u
.ends

.subckt INV1 IN OUT VDD VSS
M1      OUT     IN          VDD     VDD     PCH      W=2U     L=1U
M2      OUT     IN          VSS     VSS     NCH      W=1U     L=1U
.ends

.subckt INV2 IN OUT VDD VSS
M1      OUT     IN          VDD     VDD     PCH      W=10U    L=2U
M2      OUT     IN          VSS     VSS     NCH      W=5U     L=2U
.ends

.subckt NOR A B OUT VDD VSS
M1      1       A           VDD     VDD     PCH      W=10U    L=2U
M2      OUT     B           1       VDD     PCH      W=10U    L=2U
M3      OUT     B           VSS     VSS     NCH      W=5U     L=2U
M4      OUT     A           VSS     VSS     NCH      W=5U     L=2U
```

```
.ends

.subckt NOVLP_CLK C C_Delayed CB_Delayed VDD VSS
X1 C CB VDD VSS INV1
X2 CB CBB VDD VSS INV2
X3 CBB CBBB VDD VSS INV1
X4 CBBB CBBBB VDD VSS INV2
R1 CBB C_Delayed 0
X7 C CBBBB CB_Delayed VDD VSS NOR
.ends

.subckt TG A B EN ENB VDD VSS
M1      A      ENB            B         VDD      PCH       W=10U      L=2U
M2      A      EN             B      VSS      NCH       W=5U       L=2U
.ends

X1 vin vref a I2U I2U_S VDD VSS comparator
X2 CLK CLK_delayed CLKB_delayed VDD VSS NOVLP_CLK
X3 CLK_delayed CLKB_delayed RESET a Q QB VDD VSS DFF
X4 Vref b Q QB VDD VSS TG

M1 b QB VSS VSS    NCH       W=5U       L=2U

vdd vdd 0 1.6
vss vss 0 -1.6

vref vref 0 0.8
vin vin 0 0.1

i01 i2u_s vss 2u
i02 vdd i2u 2u

Vclk  CLK  0      pulse(-1.6v 1.6v    1.1us 0.01us 0.01us 0.13us 0.26us)
Vreset      RESET      0      pulse(-1.6v 1.6v    0us 0.01us 0.01us 1us 20ms)

.tran 10ns          30us

.END
```

Vin=0.1V

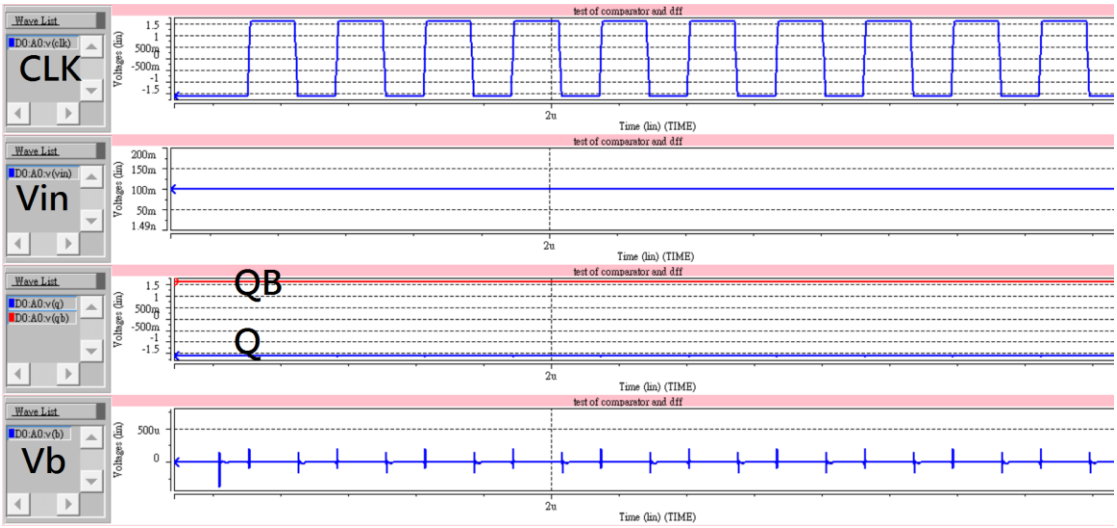


Fig. 25.3-3 The results of Experiment 25.3-1 for Vin=0.1V

Since Vin=0.1V, Q is negative, Vb is 0.

Fig. 25.3-4 shows the result of the testin when Vin=1.0V.

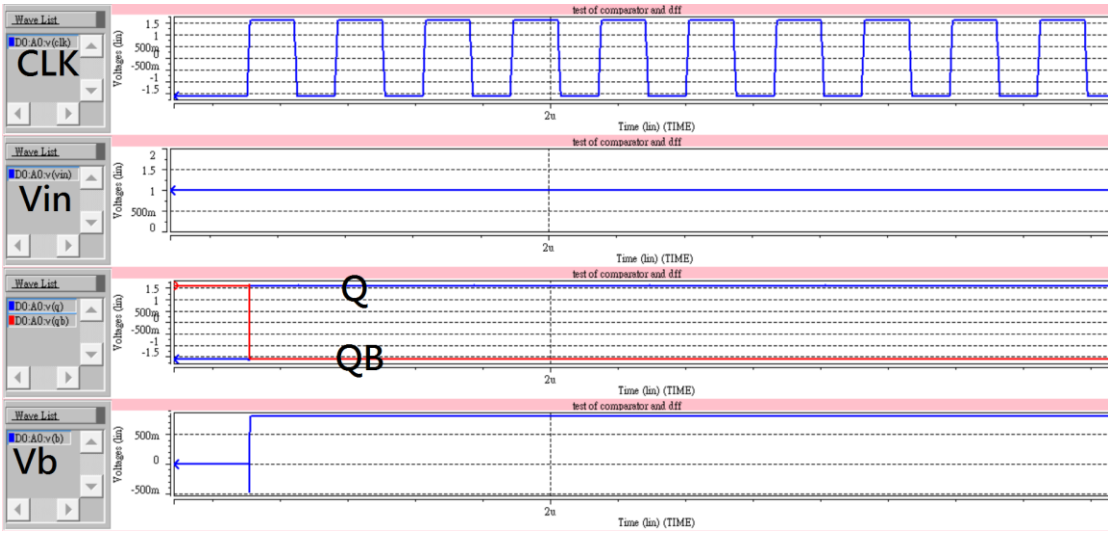
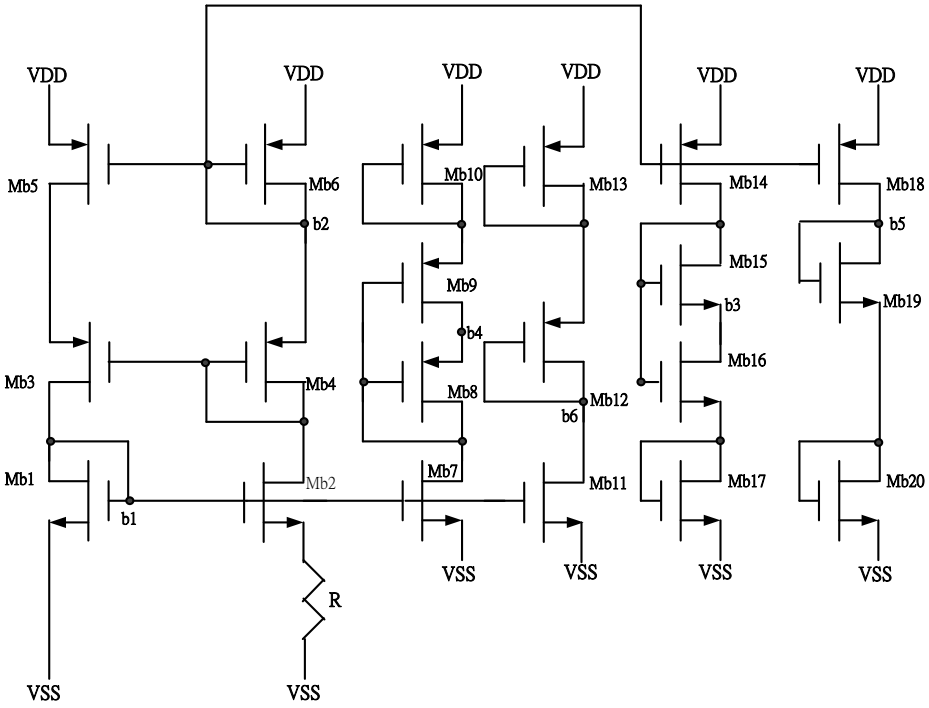


Fig. 25.3-4 The results of Experiment 25.3-1 for Vin=1.0V.

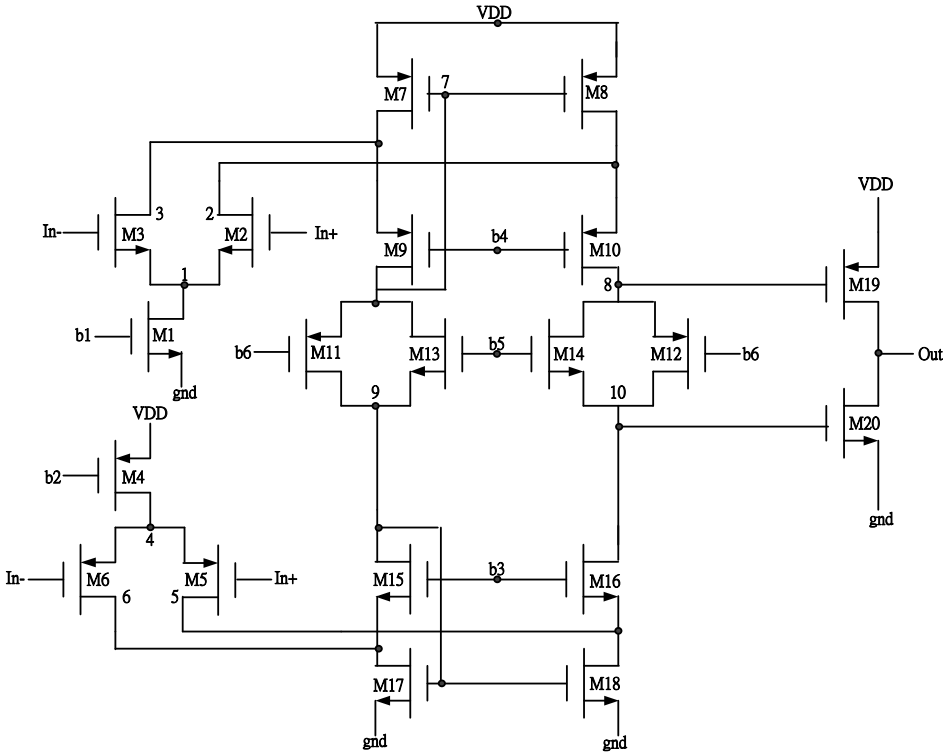
Since Vin=1.0V, Q is positive, Vb is Vref/2=0.8V.

Section 25.4 The Subtractor Circuit

The subtractor uses an OP, but this OP must be a rail to rail OP. We introduced this OP in Chapter 8 before. The circuit contains two parts. One part contains the circuit giving all of the voltage sources as shown in Fig. 25.4-1(a). The other is the rail to rail OP shown in Fig. 25.4-1(b).



(a)



(b)

Fig. 25.4-1 The rail to rail OP

Fig. 25.4-2 shows the subtractor and multiply by two circuit which we will use in our ADC circuit.

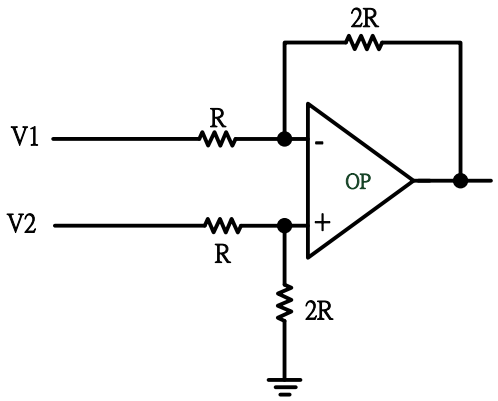


Fig. 25.4-2 The subtractor and multiply by two circuit

Experiment 25.4-1 The Testing of the subtractor and Multiply by Two Circuit

The program is in Table. 25.4-1. In the first test, V1 = 0.8V and V2 = 1.0V. The results are in Fig. 25.4-3.

Table 25.4-1 The program of Experiment 25.4-1

```
Subtractor
.protect
.LIB "D:\model\tsmc\MIXED035\mm0355v.l" TT
.unprotect
.op
.options nomod post

VDD VDD     0       1.6V
VSS  VSS     0       -1.6V

.subckt bias b1 b2 b3 b4 b5 b6 VDD VSS
R_bias     b7    VSS  0.5K

Mb1 b1    b1    VSS  VSS  NCH W=10U    L=1U
Mb2 b8    b1    b7    VSS  NCH W=10U    L=1U

Mb3 b1    b8    b9    VDD PCH  W=20U    L=1U
Mb5 b9    b2    VDD VDD PCH  W=20U    L=1U

Mb4 b8    b8    b2    VDD PCH  W=20U    L=1U
Mb6 b2    b2    VDD VDD PCH  W=20U    L=1U

Mb8 b10  b10  b4    VDD PCH  W=20U    L=1U
Mb9 b4    b10  b11  VDD PCH  W=20U    L=1U
Mb10      b11  b11  VDD VDD PCH  W=20U    L=1U
Mb12      b6    b6    b12  VDD PCH  W=20U    L=1U
Mb13      b12  b12  VDD VDD PCH  W=20U    L=1U

Mb7 b10  b1    VSS  VSS  NCH W=10U    L=1U
Mb11      b6    b1    VSS  VSS  NCH W=10U    L=1U

Mb15      b13  b13  b3    VSS  NCH W=10U    L=1U
Mb16      b3    b13  b14  VSS  NCH W=10U    L=1U
Mb17      b14  b14  VSS  VSS  NCH W=10U    L=1U
Mb19      b5    b5    b15  VSS  NCH W=10U    L=1U
Mb20      b15  b15  VSS  VSS  NCH W=10U    L=1U
```

```
Mb14      b13  b2    VDD VDD PCH  W=20U    L=1U
Mb18      b5    b2    VDD VDD PCH  W=20U    L=1U
.ends

.subckt opamp in+ in- out b1 b2 b3 b4 b5 b6 VDD VSS
M1 1 b1 VSS VSS NCH     W=10U    L=1U
M2 2 in+ 1 VSS NCH       W=10U    L=1U
M3 3 in- 1 VSS NCH W=10U    L=1U

M4 4 b2 VDD VDD PCH   W=20U    L=1U
M5 5 in+ 4 VDD PCH       W=20U    L=1U
M6 6 in- 4 VDD PCH       W=20U    L=1U

M7 3 7 VDD VDD PCH     W=20U    L=1U
M8 2 7 VDD VDD PCH     W=20U    L=1U
M9 7 b4 3 VDD PCH       W=20U    L=1U
M10 8 b4 2 VDD PCH     W=20U    L=1U

M11 9 b6 7 VDD PCH     W=20U    L=1U
M12 10 b6 8 VDD PCH    W=20U    L=1U
M13 7 b5 9 VSS NCH      W=10U    L=1U
M14 8 b5 10 VSS NCH    W=10U    L=1U

M15 9 b3 6 VSS NCH      W=10U    L=1U
M16 10 b3 5 VSS NCH    W=10U    L=1U
M17 6 9 VSS VSS NCH    W=10U    L=1U
M18 5 9 VSS VSS NCH    W=10U    L=1U

M19 out 8 VDD VDD PCH       W=20U    L=1U
M20 out 10 VSS VSS NCH       W=10U    L=1U
.ends

X1 in+ in- out b1 b2 b3 b4 b5 b6 VDD VSS opamp
X2 b1 b2 b3 b4 b5 b6 VDD VSS bias

V1 V1 0 0.8V
V2 V2 0 1.0V
```

```
R1 V2 in+ 10K
R2 in+ 0 20K
R3 V1 in- 10K
R4 in- out 20K

.tran 10p 100n

.end
```

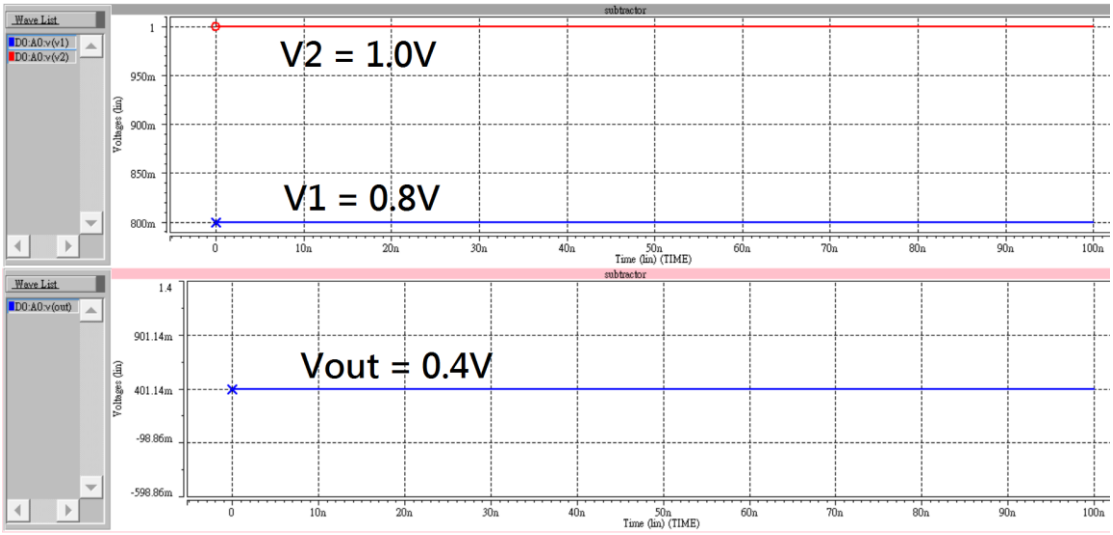


Fig. 25.4-3 The results of Experiment 25.4-1 for V1 = 0.8V, V2 = 1.0V

As can be seen, Vout = (V2 – V1) * 2 = 0.4V which is correct.

We then test the case where V1=0V and V2=0.1V. The results are in Fig. 25.4-4.

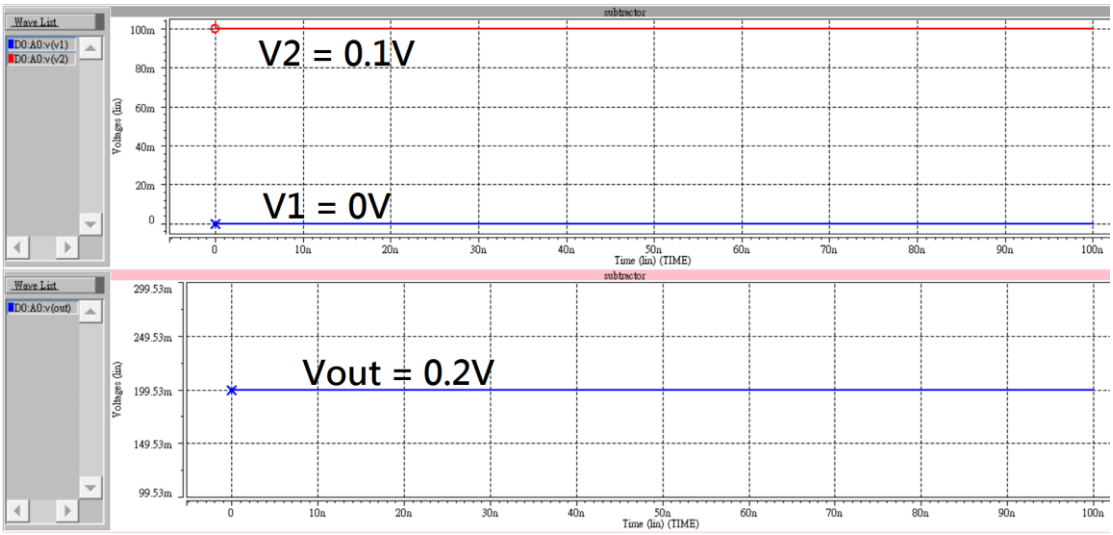


Fig. 25.4-4 The results of Experiment 25.4-1 for V1 = 0V, V2 =0. 1V

As can be seen, Vout = (V2 – V1) * 2 = 0.2V which is correct.

Fig. 25.4-5 shows the result when V1 = 0.8V, V2 = 1.6V.

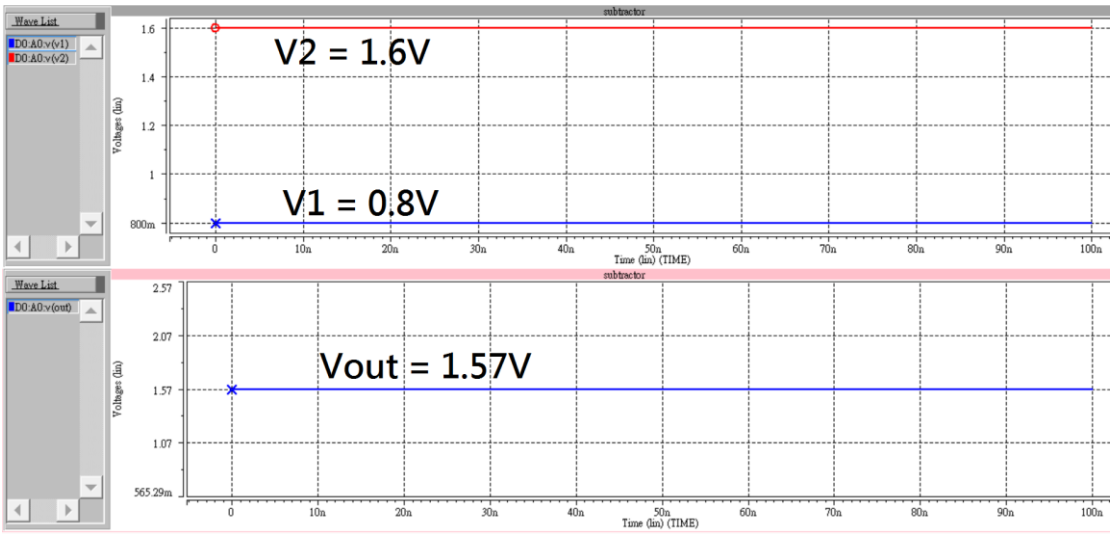


Fig. 25.4-5 The results of Experiment 25.4-1 for V1 = 0.8V, V2 = 1.6V

As can be seen, Vout = (V2 – V1) * 2 = 1.6V which is correct.

Section 25.5 The Complete One Stage

In this section, we test the complete one stage circuit of the Pipeline ADC as shown in Fig. 25.5-1..

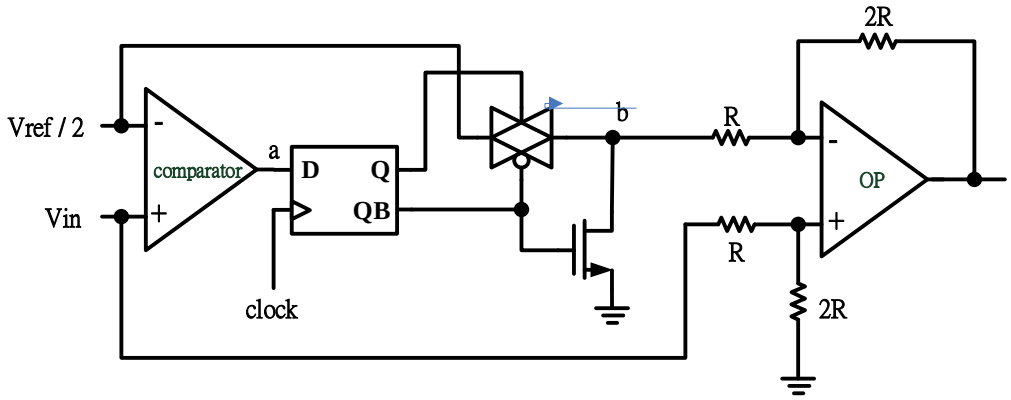
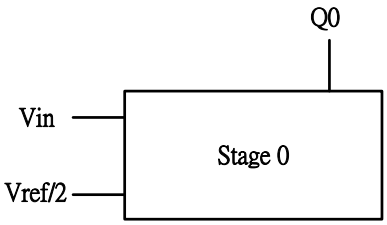


Fig. 25.5-1 The complete one stage circuit of the Pipeline ADC



Experiment 25.5-1 The Testing of the One Stage Pipeline ADC

The program of this experiment is in Table 25.5-1. The transmission gate and transistor M1 should be large enough to avoid voltage drop on the transmission gate and the transistor. For the first test, Vin=1.0V. The results are in Fig. 25.5-3.

Table 25.5-1 The program for Experiment 25.5-1

```
A stage of pipeline ADC
.protect
.LIB “D:\model\tsmc\MIXED035\mm0355v.l” TT
.unprotect
.op
.options nomod post

VDD VDD      0       1.6V
```

```
VSS  VSS     0       -1.6V

.subckt comparator INP INN VOUT I2U I2U_S VDD VSS
M6         N1N322 N1N322 VSS VSS    NCH L=2U W=3U M=2
M3         N1N320 N1N320 VSS VSS    NCH L=2U W=3U M=2
M8         VVG I2U_S VDD VDD    PCH L=5U W=6U M=2
M1       N1N320 INN VVG VDD    PCH L=2U W=6U M=2
M2       N1N322 INP VVG VDD    PCH L=2U W=6U M=2
M7         I2U_S I2U_S VDD VDD    PCH L=5U W=6U M=2
M5     N1N365 N1N322 VSS VSS    NCH L=2U W=3U M=2
M4     N1N362 N1N320 VSS VSS    NCH L=2U W=3U M=2

M10     N1N362 INP N1N372 VSS    NCH L=2U W=3U M=2
M11     I2U I2U VSS VSS    NCH L=5U W=5U M=2
M12     N1N372 I2U VSS VSS    NCH L=5U W=5U M=2
M9     N1N365 INN N1N372 VSS    NCH L=2U W=3U M=2
M14     N1N362 N1N362 VDD VDD    PCH L=2U W=6U M=2
M13     N1N365 N1N365 VDD VDD    PCH L=2U W=6U M=2

M17     N1N431 N1N365 VDD VDD    PCH L=2U W=6U M=2
M18     VOUT N1N362 VDD VDD    PCH L=2U W=6U M=2
M15     N1N431 N1N431 VSS VSS    NCH L=2U W=3U M=2
M16     VOUT N1N431 VSS VSS    NCH L=2U W=3U M=2
.ends

.subckt DFF CLK CLKB RESET D Q QB VDD VSS
MR1        RESETB   RESET      VSS  VSS   NCH W=5u      L=1u
MR2 RESETB    RESET      VDD VDD PCH  W=5u      L=1u

M1         D      CLKB       1      VSS   NCH W=5u      L=1u
MR3        1      RESETB    2      VSS   NCH W=5u      L=1u

MR4        2      RESET      VSS  VSS   NCH W=5u      L=1u

MG11      3      2      VDD VDD PCH  W=5u      L=1u
MG12      3      2      VSS  VSS   NCH W=5u      L=1u
MG13      4      3      VDD VDD PCH  W=5u      L=1u
MG14      4      3      VSS  VSS   NCH W=5u      L=1u
```

```
M2      4    CLK  5    VSS  NCH W=5u    L=1u
MR5     5    RESETB  2    VSS  NCH W=5u    L=1u

M3      4    CLK  6    VSS  NCH W=5u    L=1u
MR6     6    RESETB  7    VSS  NCH W=5u    L=1u

MR7     7    RESET    VSS  VSS  NCH W=5u    L=1u

MG21    9    7    VDD VDD PCH  W=5u    L=1u
MG22    9    7    VSS  VSS  NCH W=5u    L=1u
MG23    Q    9    VDD VDD PCH  W=5u    L=1u
MG24    Q    9    VSS  VSS  NCH W=5u    L=1u

M4      Q    CLKB     8    VSS  NCH W=5u    L=1u
MR8     7    RESETB  8    VSS  NCH W=5u    L=1u

MINV1   QB       Q        VSS VSS  NCH W=5u    L=1u
MINV2   QB       Q        VDD      VDD PCH  W=5u    L=1u
.ends

.subckt INV1 IN OUT VDD VSS
M1      OUT     IN       VDD     VDD     PCH      W=2U     L=1U
M2      OUT     IN       VSS     VSS     NCH      W=1U     L=1U
.ends

.subckt INV2 IN OUT VDD VSS
M1      OUT     IN       VDD     VDD     PCH      W=10U    L=2U
M2      OUT     IN       VSS     VSS     NCH      W=5U     L=2U
.ends

.subckt NOR A B OUT VDD VSS
M1      1       A        VDD     VDD     PCH      W=10U    L=2U
M2      OUT     B        1       VDD     PCH      W=10U    L=2U
M3      OUT     B        VSS     VSS     NCH      W=5U     L=2U
M4      OUT     A        VSS     VSS     NCH      W=5U     L=2U
.ends
```

```
.subckt NOVLP_CLK C C_Delayed CB_Delayed VDD VSS
X1 C CB VDD VSS INV1
X2 CB CBB VDD VSS INV2
X3 CBB CBBB VDD VSS INV1
X4 CBBB CBBBB VDD VSS INV2
R1 CBB C_Delayed 0
X7 C CBBBB CB_Delayed VDD VSS NOR
.ends

.subckt TG A B EN ENB VDD VSS
M1      A     ENB          B        VDD     PCH      W=100U     L=2U
M2      A     EN           B      VSS     NCH      W=50U      L=2U
.ends

.subckt bias b1 b2 b3 b4 b5 b6 VDD VSS
R_bias     b7    VSS  0.5K

Mb1 b1    b1    VSS  VSS  NCH W=10U    L=1U
Mb2 b8    b1    b7    VSS  NCH W=10U    L=1U

Mb3 b1    b8    b9    VDD PCH  W=20U    L=1U
Mb5 b9    b2    VDD VDD PCH  W=20U    L=1U

Mb4 b8    b8    b2    VDD PCH  W=20U    L=1U
Mb6 b2    b2    VDD VDD PCH  W=20U    L=1U

Mb8 b10  b10  b4    VDD PCH  W=20U    L=1U
Mb9 b4    b10  b11  VDD PCH  W=20U    L=1U
Mb10      b11  b11  VDD VDD PCH  W=20U    L=1U
Mb12      b6    b6    b12  VDD PCH  W=20U    L=1U
Mb13      b12  b12  VDD VDD PCH  W=20U    L=1U

Mb7 b10  b1    VSS  VSS  NCH W=10U    L=1U
Mb11      b6    b1    VSS  VSS  NCH W=10U    L=1U

Mb15      b13  b13  b3    VSS  NCH W=10U    L=1U
Mb16      b3    b13  b14  VSS  NCH W=10U    L=1U
Mb17      b14  b14  VSS  VSS  NCH W=10U    L=1U
```

```
Mb19     b5   b5   b15  VSS  NCH W=10U   L=1U
Mb20     b15  b15  VSS  VSS  NCH W=10U   L=1U

Mb14     b13  b2   VDD VDD PCH  W=20U   L=1U
Mb18     b5   b2   VDD VDD PCH  W=20U   L=1U
.ends

.subckt opamp in+ in- out b1 b2 b3 b4 b5 b6 VDD VSS
M1 1 b1 VSS VSS NCH    W=10U   L=1U
M2 2 in+ 1 VSS NCH     W=10U   L=1U
M3 3 in- 1 VSS NCH W=10U   L=1U

M4 4 b2 VDD VDD PCH  W=20U   L=1U
M5 5 in+ 4 VDD PCH     W=20U   L=1U
M6 6 in- 4 VDD PCH     W=20U   L=1U

M7 3 7 VDD VDD PCH     W=20U   L=1U
M8 2 7 VDD VDD PCH     W=20U   L=1U
M9 7 b4 3 VDD PCH      W=20U   L=1U
M10 8 b4 2 VDD PCH     W=20U   L=1U

M11 9 b6 7 VDD PCH     W=20U   L=1U
M12 10 b6 8 VDD PCH    W=20U   L=1U
M13 7 b5 9 VSS NCH     W=10U   L=1U
M14 8 b5 10 VSS NCH    W=10U   L=1U

M15 9 b3 6 VSS NCH     W=10U   L=1U
M16 10 b3 5 VSS NCH    W=10U   L=1U
M17 6 9 VSS VSS NCH    W=10U   L=1U
M18 5 9 VSS VSS NCH    W=10U   L=1U

M19 out 8 VDD VDD PCH      W=20U   L=1U
M20 out 10 VSS VSS NCH     W=10U   L=1U
.ends

X1 vin vref a I2U I2U_S VDD VSS comparator
X2 CLK CLK_delayed CLKB_delayed VDD VSS NOVLP_CLK
X3 CLK_delayed CLKB_delayed RESET a Q QB VDD VSS DFF
```

```
X4 Vref b Q QB VDD VSS TG
X5 in+ in- out b1 b2 b3 b4 b5 b6 VDD VSS opamp
X6 b1 b2 b3 b4 b5 b6 VDD VSS bias

R1 vin in+ 20K
R2 in+ 0 40K
R3 b in- 20K
R4 in- out 40K

M1 b QB GND GND    NCH        W=50U        L=2U

i01 i2u_s vss 2u
i02 vdd i2u 2u

vref vref 0 0.8
vin vin 0 0.4

Vclk  CLK  0      pulse(-1.6v 1.6v    1.1us 0.01us 0.01us 0.13us 0.26us)
Vreset      RESET      0      pulse(-1.6v 1.6v    0us 0.01us 0.01us 1us 20ms)

.tran 10ns          30us

.end
```

Vin = 1.0V

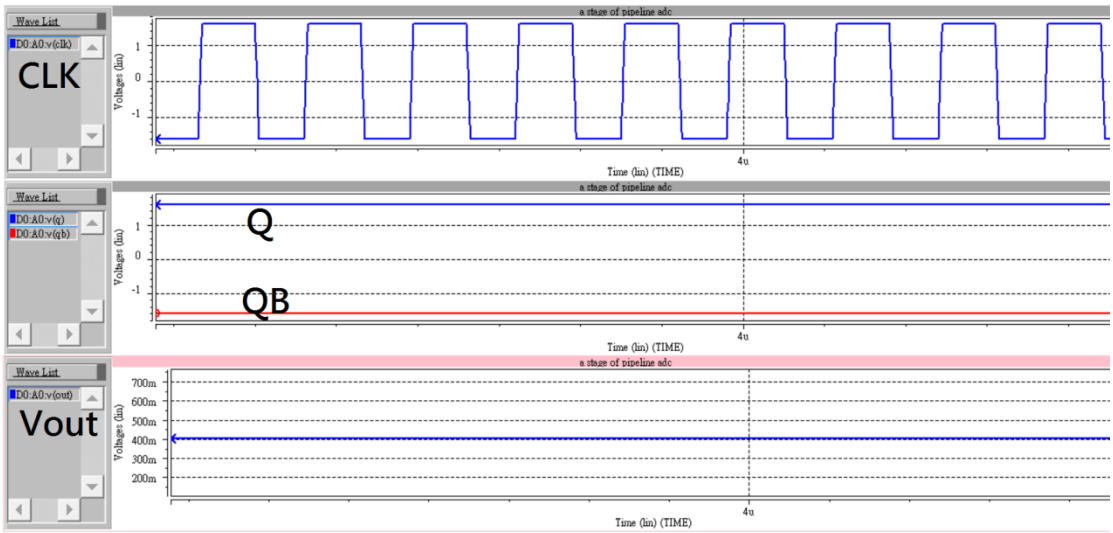
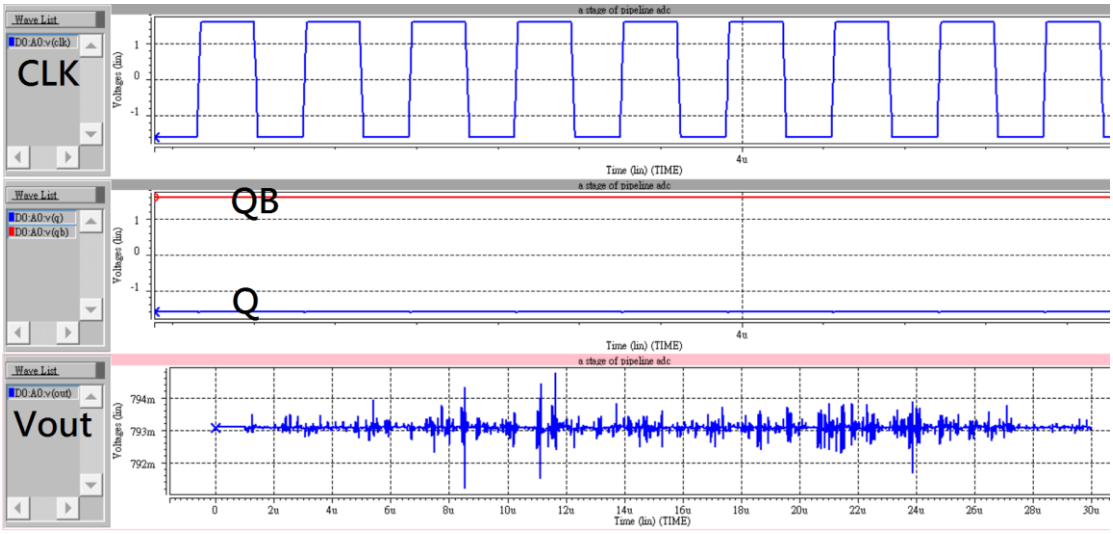


Fig. 25.5-3 The results of Experiment 25.5-1 when Vin=1.0V

Since Vin=1.0V is larger than Vref/2=0.8V, Q0= high and Vout = (1.0 – 0.8) * 2 = 0.4V.

The results of Vin = 0.4V is shown Fig. 25.5-4.



Since Vin=1.0V is smaller than Vref/2=0.8V, Q0= high and Vout = (1.0 – 0.8) * 2 = 0.4V.

Section 25.6. Two Stage Pipeline ADC

In this section, we assume that the output of the ADC needs two bits, For the Pipeline ADC, it therefore needs two stages as shown in Fig. 25.6-1

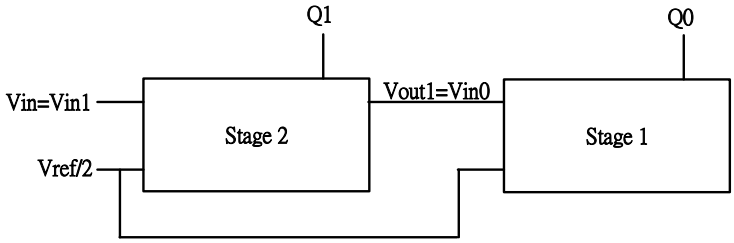


Fig. 25.6-1 A two stage Pipleline ADC.

Experiment 25.6-1 The Testing of the Two Stage Pipeline ADC.

The program is in Table 25.6-1. For the first test, Vin=1.0V. The results are in Fig. 25.6-2..

Table 25.6-1 The program for Experiment 25.6-1

```
Two stages
.protect
.LIB "D:\model\tsmc\MIXED035\mm0355v.l" TT
.unprotect
.op
.options nomod post

VDD VDD      0       1.6V
VSS  VSS     0       -1.6V

.subckt comparator INP INN VOUT I2U I2U_S VDD VSS
M6          N1N322 N1N322 VSS VSS    NCH L=2U W=3U M=2
M3          N1N320 N1N320 VSS VSS    NCH L=2U W=3U M=2
M8          VVG I2U_S VDD VDD    PCH L=5U W=6U M=2
M1        N1N320 INN VVG VDD    PCH L=2U W=6U M=2
M2        N1N322 INP VVG VDD    PCH L=2U W=6U M=2
M7          I2U_S I2U_S VDD VDD    PCH L=5U W=6U M=2
M5      N1N365 N1N322 VSS VSS    NCH L=2U W=3U M=2
M4      N1N362 N1N320 VSS VSS    NCH L=2U W=3U M=2
```

```
M10     N1N362 INP N1N372 VSS    NCH L=2U W=3U M=2
M11     I2U I2U VSS VSS    NCH L=5U W=5U M=2
M12     N1N372 I2U VSS VSS    NCH L=5U W=5U M=2
M9     N1N365 INN N1N372 VSS    NCH L=2U W=3U M=2
M14     N1N362 N1N362 VDD VDD    PCH L=2U W=6U M=2
M13     N1N365 N1N365 VDD VDD    PCH L=2U W=6U M=2

M17     N1N431 N1N365 VDD VDD    PCH L=2U W=6U M=2
M18     VOUT N1N362 VDD VDD    PCH L=2U W=6U M=2
M15     N1N431 N1N431 VSS VSS    NCH L=2U W=3U M=2
M16     VOUT N1N431 VSS VSS    NCH L=2U W=3U M=2
.ends

.subckt DFF CLK CLKB RESET D Q QB VDD VSS
MR1       RESETB  RESET     VSS  VSS  NCH W=5u     L=1u
MR2 RESETB    RESET     VDD VDD PCH  W=5u     L=1u

M1       D     CLKB      1     VSS  NCH W=5u     L=1u
MR3      1     RESETB    2     VSS  NCH W=5u     L=1u

MR4      2     RESET     VSS  VSS  NCH W=5u     L=1u

MG11     3     2     VDD VDD PCH  W=5u     L=1u
MG12     3     2     VSS  VSS  NCH W=5u     L=1u
MG13     4     3     VDD VDD PCH  W=5u     L=1u
MG14     4     3     VSS  VSS  NCH W=5u     L=1u

M2       4     CLK  5     VSS  NCH W=5u     L=1u
MR5      5     RESETB    2     VSS  NCH W=5u     L=1u

M3       4     CLK  6     VSS  NCH W=5u     L=1u
MR6      6     RESETB    7     VSS  NCH W=5u     L=1u

MR7      7     RESET     VSS  VSS  NCH W=5u     L=1u

MG21     9     7     VDD VDD PCH  W=5u     L=1u
MG22     9     7     VSS  VSS  NCH W=5u     L=1u
```

```
MG23     Q    9     VDD VDD PCH  W=5u     L=1u
MG24     Q    9     VSS  VSS  NCH W=5u     L=1u

M4       Q    CLKB      8     VSS  NCH W=5u     L=1u
MR8      7    RESETB    8     VSS  NCH W=5u     L=1u

MINV1    QB         Q          VSS VSS  NCH W=5u     L=1u
MINV2    QB         Q          VDD      VDD PCH  W=5u     L=1u
.ends

.subckt INV1 IN OUT VDD VSS
M1      OUT     IN          VDD     VDD     PCH      W=2U     L=1U
M2      OUT     IN          VSS     VSS     NCH      W=1U     L=1U
.ends

.subckt INV2 IN OUT VDD VSS
M1      OUT     IN          VDD     VDD     PCH      W=10U    L=2U
M2      OUT     IN          VSS     VSS     NCH      W=5U     L=2U
.ends

.subckt NOR A B OUT VDD VSS
M1      1       A           VDD     VDD     PCH      W=10U    L=2U
M2      OUT     B           1       VDD     PCH      W=10U    L=2U
M3      OUT     B           VSS     VSS     NCH      W=5U     L=2U
M4      OUT     A           VSS     VSS     NCH      W=5U     L=2U
.ends

.subckt NOVLP_CLK C C_Delayed CB_Delayed VDD VSS
X1 C CB VDD VSS INV1
X2 CB CBB VDD VSS INV2
X3 CBB CBBB VDD VSS INV1
X4 CBBB CBBBB VDD VSS INV2
R1 CBB C_Delayed 0
X7 C CBBBB CB_Delayed VDD VSS NOR
.ends

.subckt TG A B EN ENB VDD VSS
M1      A    ENB          B       VDD     PCH      W=100U    L=2U
```

```
M2      A      EN          B      VSS      NCH       W=50U       L=2U
.ends

.subckt bias b1 b2 b3 b4 b5 b6 VDD VSS
R_bias     b7    VSS  0.5K

Mb1 b1    b1    VSS  VSS  NCH W=10U    L=1U
Mb2 b8    b1    b7    VSS  NCH W=10U    L=1U

Mb3 b1    b8    b9    VDD PCH  W=20U    L=1U
Mb5 b9    b2    VDD VDD PCH  W=20U    L=1U

Mb4 b8    b8    b2    VDD PCH  W=20U    L=1U
Mb6 b2    b2    VDD VDD PCH  W=20U    L=1U

Mb8 b10  b10  b4    VDD PCH  W=20U    L=1U
Mb9 b4    b10  b11  VDD PCH  W=20U    L=1U
Mb10      b11  b11  VDD VDD PCH  W=20U    L=1U
Mb12      b6    b6    b12  VDD PCH  W=20U    L=1U
Mb13      b12  b12  VDD VDD PCH  W=20U    L=1U

Mb7 b10  b1    VSS  VSS  NCH W=10U    L=1U
Mb11      b6    b1    VSS  VSS  NCH W=10U    L=1U

Mb15      b13  b13  b3    VSS  NCH W=10U    L=1U
Mb16      b3    b13  b14  VSS  NCH W=10U    L=1U
Mb17      b14  b14  VSS  VSS  NCH W=10U    L=1U
Mb19      b5    b5    b15  VSS  NCH W=10U    L=1U
Mb20      b15  b15  VSS  VSS  NCH W=10U    L=1U

Mb14      b13  b2    VDD VDD PCH  W=20U    L=1U
Mb18      b5    b2    VDD VDD PCH  W=20U    L=1U
.ends

.subckt opamp in+ in- out b1 b2 b3 b4 b5 b6 VDD VSS
M1 1 b1 VSS VSS NCH     W=10U    L=1U
M2 2 in+ 1 VSS NCH       W=10U    L=1U
M3 3 in- 1 VSS NCH W=10U    L=1U
```

```
M4 4 b2 VDD VDD PCH   W=20U    L=1U
M5 5 in+ 4 VDD PCH    W=20U    L=1U
M6 6 in- 4 VDD PCH    W=20U    L=1U

M7 3 7 VDD VDD PCH    W=20U    L=1U
M8 2 7 VDD VDD PCH    W=20U    L=1U
M9 7 b4 3 VDD PCH     W=20U    L=1U
M10 8 b4 2 VDD PCH    W=20U    L=1U

M11 9 b6 7 VDD PCH    W=20U    L=1U
M12 10 b6 8 VDD PCH   W=20U    L=1U
M13 7 b5 9 VSS NCH    W=10U    L=1U
M14 8 b5 10 VSS NCH   W=10U    L=1U

M15 9 b3 6 VSS NCH    W=10U    L=1U
M16 10 b3 5 VSS NCH   W=10U    L=1U
M17 6 9 VSS VSS NCH   W=10U    L=1U
M18 5 9 VSS VSS NCH   W=10U    L=1U

M19 out 8 VDD VDD PCH      W=20U    L=1U
M20 out 10 VSS VSS NCH     W=10U    L=1U
.ends

.subckt stage Vin Vref out CLK RESET Q VDD VSS
X1 vin vref a I2U I2U_S VDD VSS comparator
X2 CLK CLK_delayed CLKB_delayed VDD VSS NOVLP_CLK
X3 CLK_delayed CLKB_delayed RESET a Q QB VDD VSS DFF
X4 Vref b Q QB VDD VSS TG
X5 in+ in- out b1 b2 b3 b4 b5 b6 VDD VSS opamp
X6 b1 b2 b3 b4 b5 b6 VDD VSS bias

R1 vin in+ 20K
R2 in+ 0 40K
R3 b in- 20K
R4 in- out 40K

M1 b QB GND GND    NCH       W=50U       L=2U
```

```
i01 i2u_s vss 2u
i02 vdd i2u 2u
.ends

X1 Vin Vref Vout1 CLK RESET Q1 VDD VSS stage
X2 Vout1 Vref Vout0 CLK RESET Q0 VDD VSS stage

vref vref 0 0.8
vin vin 0 0.6

Vclk  CLK  0      pulse(-1.6v 1.6v    1.1us 0.01us 0.01us 0.13us 0.26us)
Vreset      RESET      0      pulse(-1.6v 1.6v    0us 0.01us 0.01us 1us 20ms)

.tran 10ns          30us

.end
```

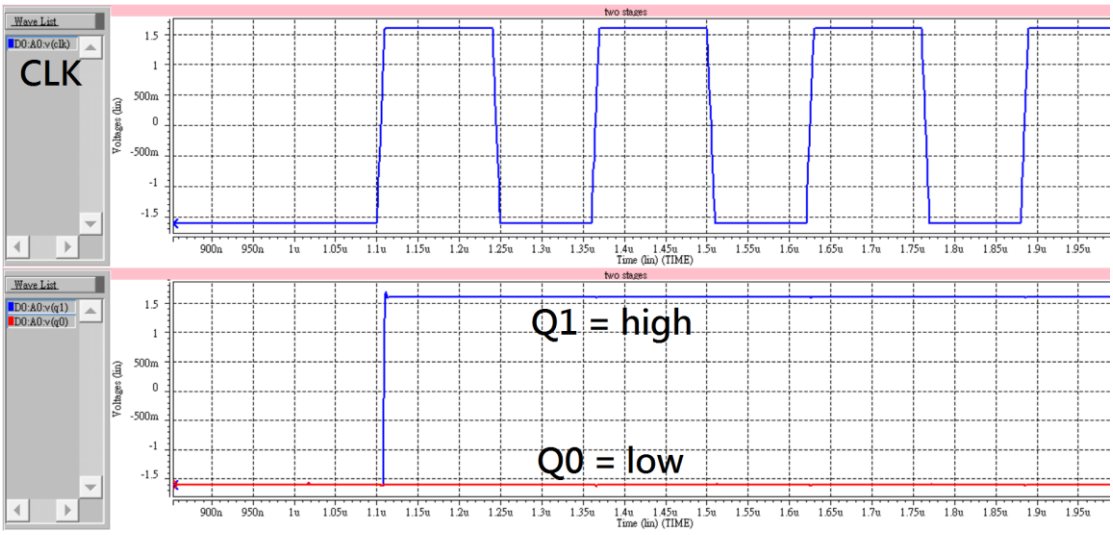


Fig. 25.6-2The results of Experiment 25.6-1 when Vin=1.0

The Output = 10 which is correct.

Fig. 25.6-3 shows the results for Vin = 1.4V.

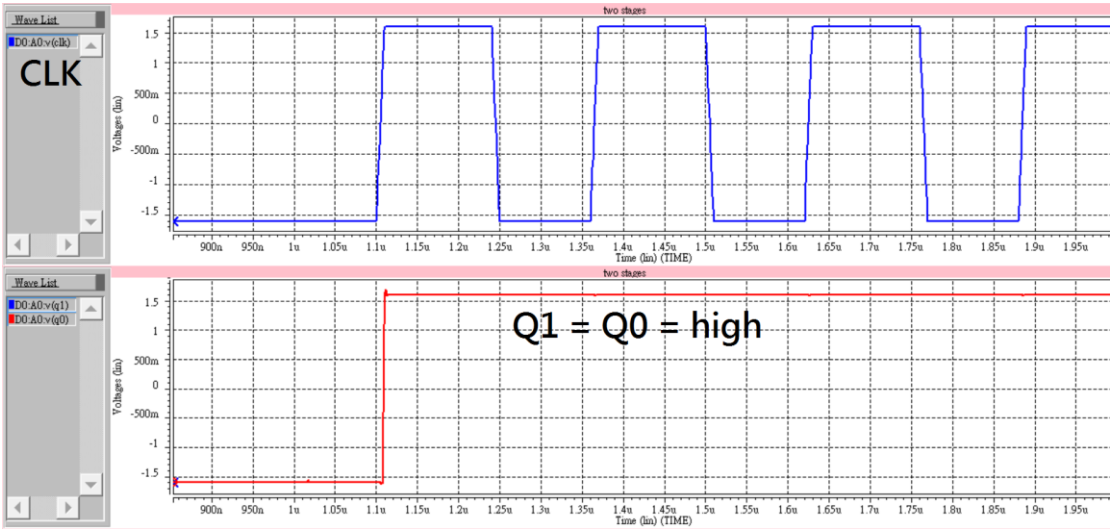


Fig. 25.6-3 The results of Experiment 25.6-3 when Vin=1.4V

The Output = 11 which is correct.

Fig. 25.6-4 shows the results for Vin = 0.3V.

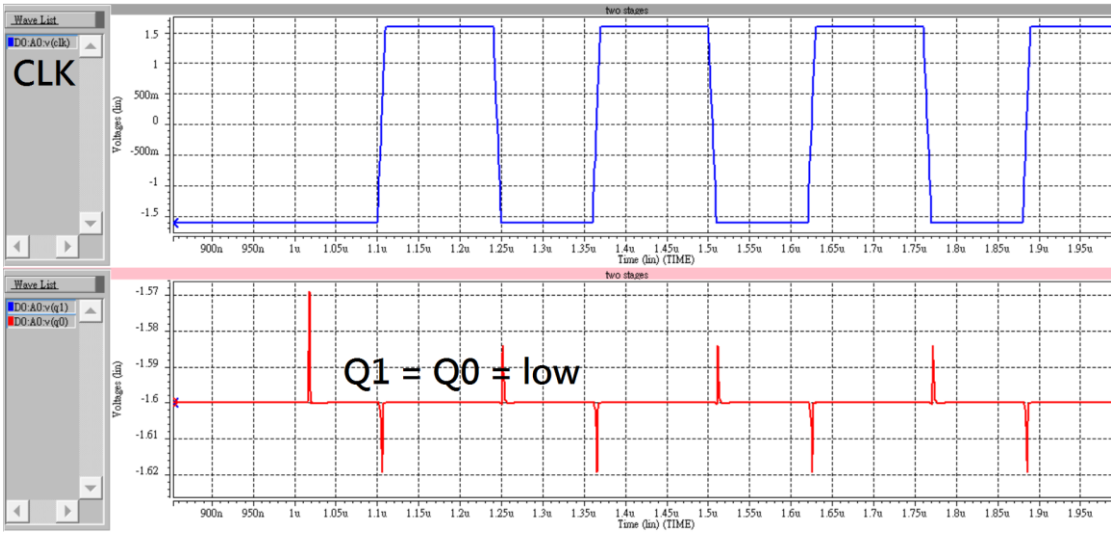


Fig. 25.6-4 The results of Experiment 25.6-3 when Vin=0.3V

The Output = 00 which is correct.

Fig. 25.6-5 shows the results for Vin = 0.6V.

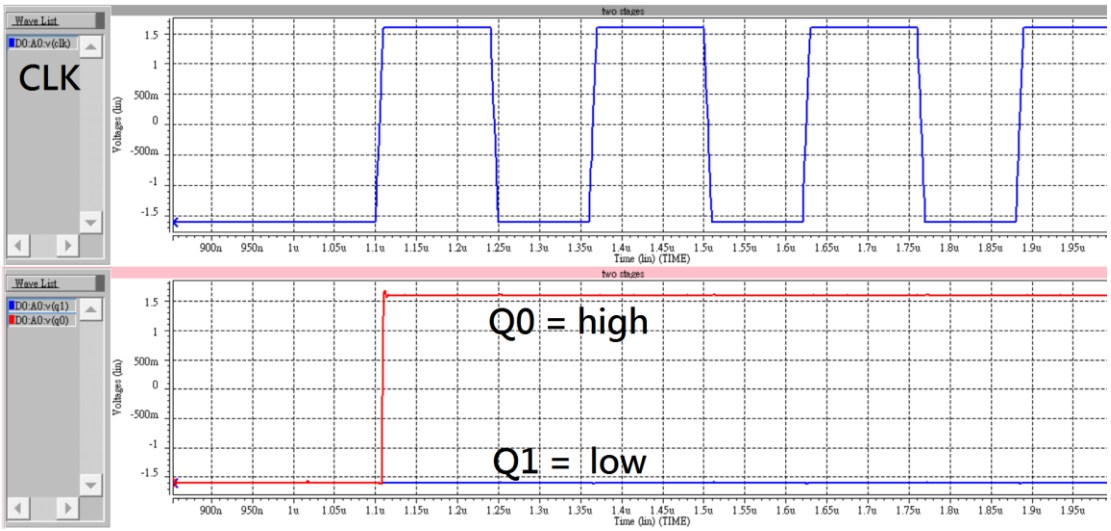


Fig. 25.6-5 The results of Experiment 25.6-3 when Vin=0.6V

The Output = 01 which is correct.

Section 25.7 Three Stage Pipeline ADC

In this section, we assume that the ADC has three bits as output.. Therefore we need three stages as shown in Fig. 25.7-1.

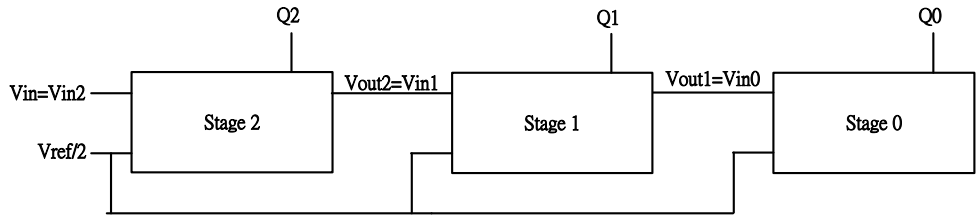


Fig. 25.7-1 The three stage Pipeline ADC

Experiment 25.7-1 The Testing of the Three Stage Pipeline ADC

The program is in Table 25.7-1. For the first test, Vin = 1.5V. The results are in Fig. 25.7-2.

Table 25.7-1 The program for Experiment 25.7-1

```
Two stages
.protect
.LIB “D:\model\tsmc\MIXED035\mm0355v.l” TT
.unprotect
.op
.options nomod post

VDD VDD      0       1.6V
VSS  VSS     0       -1.6V

.subckt comparator INP INN VOUT I2U I2U_S VDD VSS
M6          N1N322 N1N322 VSS VSS    NCH L=2U W=3U M=2
M3          N1N320 N1N320 VSS VSS    NCH L=2U W=3U M=2
M8          VVG I2U_S VDD VDD    PCH L=5U W=6U M=2
M1        N1N320 INN VVG VDD    PCH L=2U W=6U M=2
M2        N1N322 INP VVG VDD    PCH L=2U W=6U M=2
M7          I2U_S I2U_S VDD VDD    PCH L=5U W=6U M=2
M5      N1N365 N1N322 VSS VSS    NCH L=2U W=3U M=2
M4      N1N362 N1N320 VSS VSS    NCH L=2U W=3U M=2

M10      N1N362 INP N1N372 VSS    NCH L=2U W=3U M=2
```

```
M11     I2U I2U VSS VSS    NCH L=5U W=5U M=2
M12     N1N372 I2U VSS VSS    NCH L=5U W=5U M=2
M9     N1N365 INN N1N372 VSS    NCH L=2U W=3U M=2
M14     N1N362 N1N362 VDD VDD    PCH L=2U W=6U M=2
M13     N1N365 N1N365 VDD VDD    PCH L=2U W=6U M=2

M17     N1N431 N1N365 VDD VDD    PCH L=2U W=6U M=2
M18     VOUT N1N362 VDD VDD    PCH L=2U W=6U M=2
M15     N1N431 N1N431 VSS VSS    NCH L=2U W=3U M=2
M16     VOUT N1N431 VSS VSS    NCH L=2U W=3U M=2
.ends

.subckt DFF CLK CLKB RESET D Q QB VDD VSS
MR1       RESETB  RESET     VSS  VSS  NCH W=5u     L=1u
MR2 RESETB    RESET     VDD VDD PCH  W=5u     L=1u

M1        D     CLKB      1     VSS  NCH W=5u     L=1u
MR3       1     RESETB    2     VSS  NCH W=5u     L=1u

MR4       2     RESET     VSS  VSS  NCH W=5u     L=1u

MG11      3     2     VDD VDD PCH  W=5u     L=1u
MG12      3     2     VSS  VSS  NCH W=5u     L=1u
MG13      4     3     VDD VDD PCH  W=5u     L=1u
MG14      4     3     VSS  VSS  NCH W=5u     L=1u

M2        4     CLK  5     VSS  NCH W=5u     L=1u
MR5       5     RESETB    2     VSS  NCH W=5u     L=1u

M3        4     CLK  6     VSS  NCH W=5u     L=1u
MR6       6     RESETB    7     VSS  NCH W=5u     L=1u

MR7       7     RESET     VSS  VSS  NCH W=5u     L=1u

MG21      9     7     VDD VDD PCH  W=5u     L=1u
MG22      9     7     VSS  VSS  NCH W=5u     L=1u
MG23      Q     9     VDD VDD PCH  W=5u     L=1u
MG24      Q     9     VSS  VSS  NCH W=5u     L=1u
```

```
M4        Q     CLKB       8     VSS  NCH W=5u      L=1u
MR8       7     RESETB     8     VSS  NCH W=5u      L=1u

MINV1     QB          Q          VSS VSS  NCH W=5u      L=1u
MINV2     QB          Q          VDD       VDD PCH  W=5u      L=1u
.ends

.subckt INV1 IN OUT VDD VSS
M1      OUT     IN          VDD     VDD     PCH       W=2U      L=1U
M2      OUT     IN          VSS     VSS     NCH       W=1U      L=1U
.ends

.subckt INV2 IN OUT VDD VSS
M1      OUT     IN          VDD     VDD     PCH       W=10U     L=2U
M2      OUT     IN          VSS     VSS     NCH       W=5U      L=2U
.ends

.subckt NOR A B OUT VDD VSS
M1      1         A           VDD     VDD     PCH       W=10U     L=2U
M2      OUT     B           1         VDD     PCH       W=10U     L=2U
M3      OUT     B           VSS     VSS     NCH       W=5U      L=2U
M4      OUT     A           VSS     VSS     NCH       W=5U      L=2U
.ends

.subckt NOVLP_CLK C C_Delayed CB_Delayed VDD VSS
X1 C CB VDD VSS INV1
X2 CB CBB VDD VSS INV2
X3 CBB CBBB VDD VSS INV1
X4 CBBB CBBBB VDD VSS INV2
R1 CBB C_Delayed 0
X7 C CBBBB CB_Delayed VDD VSS NOR
.ends

.subckt TG A B EN ENB VDD VSS
M1      A     ENB          B        VDD     PCH       W=100U     L=2U
M2      A     EN          B     VSS     NCH       W=50U      L=2U
.ends
```

```
.subckt bias b1 b2 b3 b4 b5 b6 VDD VSS
R_bias     b7    VSS  0.5K

Mb1 b1    b1    VSS  VSS  NCH W=10U    L=1U
Mb2 b8    b1    b7   VSS  NCH W=10U    L=1U

Mb3 b1    b8    b9   VDD PCH  W=20U    L=1U
Mb5 b9    b2    VDD VDD PCH  W=20U    L=1U

Mb4 b8    b8    b2   VDD PCH  W=20U    L=1U
Mb6 b2    b2    VDD VDD PCH  W=20U    L=1U

Mb8 b10   b10   b4   VDD PCH  W=20U    L=1U
Mb9 b4    b10   b11  VDD PCH  W=20U    L=1U
Mb10      b11   b11  VDD VDD PCH  W=20U    L=1U
Mb12      b6    b6   b12  VDD PCH  W=20U    L=1U
Mb13      b12   b12  VDD VDD PCH  W=20U    L=1U

Mb7 b10   b1    VSS  VSS  NCH W=10U    L=1U
Mb11      b6    b1   VSS  VSS  NCH W=10U    L=1U

Mb15      b13   b13  b3   VSS  NCH W=10U    L=1U
Mb16      b3    b13  b14  VSS  NCH W=10U    L=1U
Mb17      b14   b14  VSS  VSS  NCH W=10U    L=1U
Mb19      b5    b5   b15  VSS  NCH W=10U    L=1U
Mb20      b15   b15  VSS  VSS  NCH W=10U    L=1U

Mb14      b13   b2   VDD VDD PCH  W=20U    L=1U
Mb18      b5    b2   VDD VDD PCH  W=20U    L=1U
.ends

.subckt opamp in+ in- out b1 b2 b3 b4 b5 b6 VDD VSS
M1 1 b1 VSS VSS NCH      W=10U    L=1U
M2 2 in+ 1 VSS NCH       W=10U    L=1U
M3 3 in- 1 VSS NCH W=10U    L=1U

M4 4 b2 VDD VDD PCH   W=20U    L=1U
```

```
M5 5 in+ 4 VDD PCH      W=20U   L=1U
M6 6 in- 4 VDD PCH      W=20U   L=1U

M7 3 7 VDD VDD PCH    W=20U   L=1U
M8 2 7 VDD VDD PCH    W=20U   L=1U
M9 7 b4 3 VDD PCH     W=20U   L=1U
M10 8 b4 2 VDD PCH    W=20U   L=1U

M11 9 b6 7 VDD PCH    W=20U   L=1U
M12 10 b6 8 VDD PCH   W=20U   L=1U
M13 7 b5 9 VSS NCH    W=10U   L=1U
M14 8 b5 10 VSS NCH   W=10U   L=1U

M15 9 b3 6 VSS NCH    W=10U   L=1U
M16 10 b3 5 VSS NCH   W=10U   L=1U
M17 6 9 VSS VSS NCH   W=10U   L=1U
M18 5 9 VSS VSS NCH   W=10U   L=1U

M19 out 8 VDD VDD PCH      W=20U   L=1U
M20 out 10 VSS VSS NCH     W=10U   L=1U
.ends

.subckt stage Vin Vref out CLK RESET Q VDD VSS
X1 vin vref a I2U I2U_S VDD VSS comparator
X2 CLK CLK_delayed CLKB_delayed VDD VSS NOVLP_CLK
X3 CLK_delayed CLKB_delayed RESET a Q QB VDD VSS DFF
X4 Vref b Q QB VDD VSS TG
X5 in+ in- out b1 b2 b3 b4 b5 b6 VDD VSS opamp
X6 b1 b2 b3 b4 b5 b6 VDD VSS bias

R1 vin in+ 20K
R2 in+ 0 40K
R3 b in- 20K
R4 in- out 40K

M1 b QB GND GND    NCH      W=50U      L=2U

i01 i2u_s vss 2u
```

```
i02 vdd i2u 2u
.ends

X1 Vin Vref Vout2 CLK RESET Q2 VDD VSS stage
X2 Vout2 Vref Vout1 CLK RESET Q1 VDD VSS stage
X3 Vout1 Vref Vout0 CLK RESET Q0 VDD VSS stage

vref vref 0 0.8
vin vin 0 1.1

Vclk  CLK  0      pulse(-1.6v 1.6v    1.1us 0.01us 0.01us 0.13us 0.26us)
Vreset      RESET      0      pulse(-1.6v 1.6v    0us 0.01us 0.01us 1us 20ms)

.tran 10ns          30us

.end
```

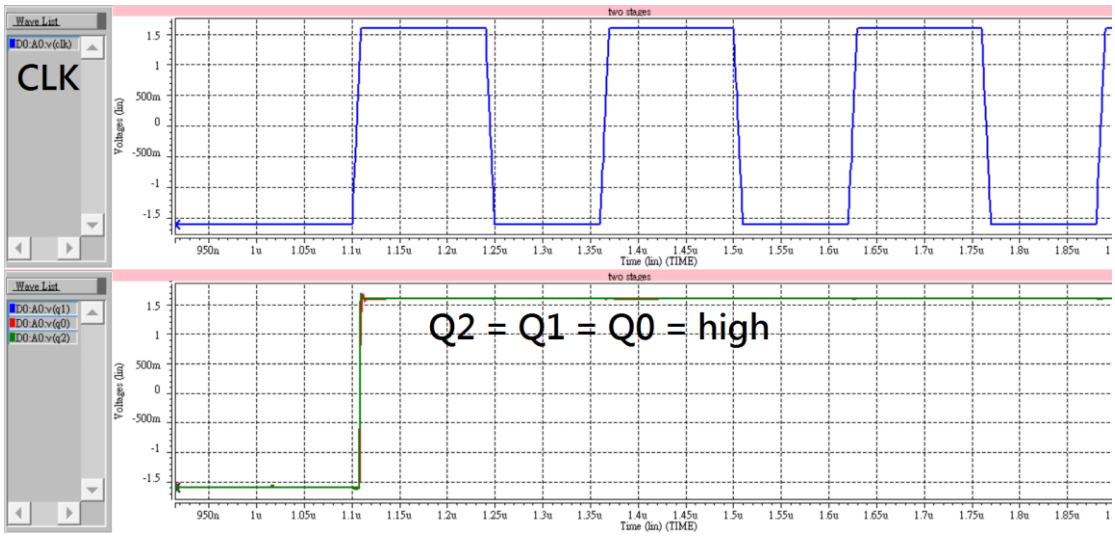


Fig. 25.7-2 The results of Experiment 25.7-1 when Vin=1.5V

The output = 111 which is correct.

Fig. 25.7-3 shows the result when Vi=0.3V.

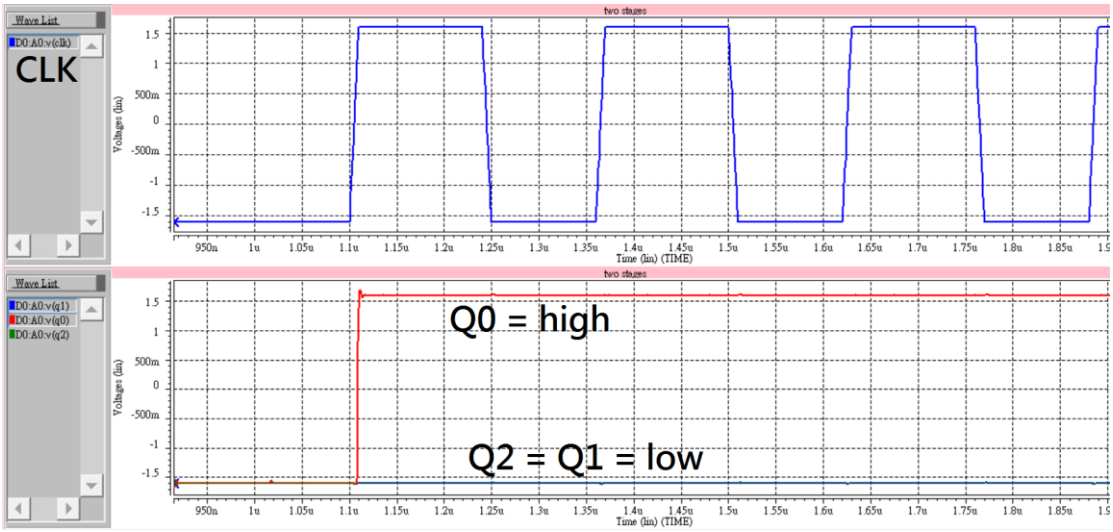


Fig. 25.7-3 The results of Experiment 25.7-1 when Vin=0.3V

The output = 001 which is correct.

Fig. 25.7-4 shows the result when Vi=1.1V.

Vin = 1.1V

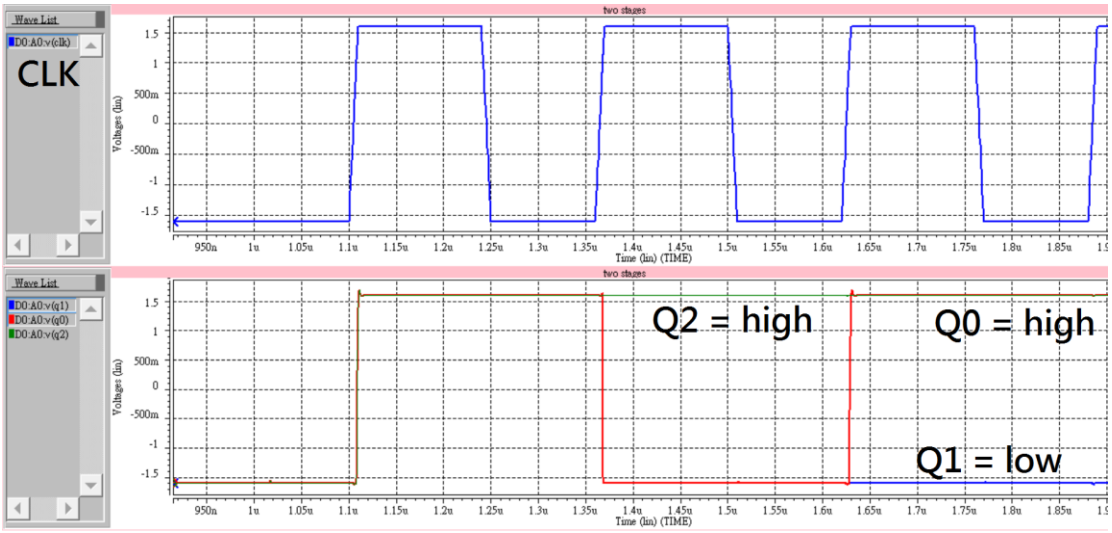


Fig. 25.7-4 The results of Experiment 25.7-1 when Vin=1.1V

The output = 101 which is correct.